CONFIDENTIAL A

PCB Design Guideline For MT6737

V0_1

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Revision History

Version	Date	Description	Editors
V0_1	2015/12/23	First release	Tina Tang, Mason Wu

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Outlines

- **Brief Introduction to MT6737**
- **Packaging**
  - Package Outline of MT6737
  - MT6737 Footprint Recommendation
  - MT6737 Ball Out Design
- **General Guidelines**
  - PCB Stack-up Recommendation
  - Common Rules and Via Type
  - Placement Notes
  - MT6737 Fan Out
- **Design Guidelines for High-Speed Digital Signals**
  - LPDDR3
  - LPDDR2
  - PDN Design
- **Others**
  - MT6737 RF Interface - MT6169 - MT6158
  - MT6328 (PMU)
  - MT6625 (BT/FM/WiFi/GPS)
  - USB/MIPI/ SIM Card/ T-Card/ eMMC/Differential Pair Layout Suggestion

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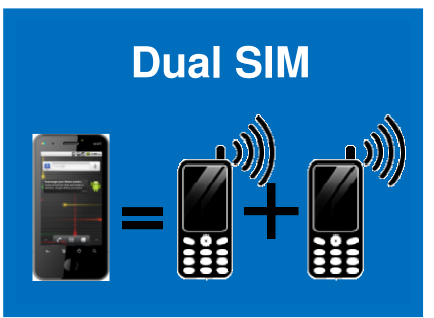
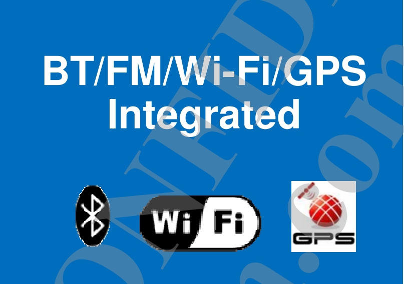
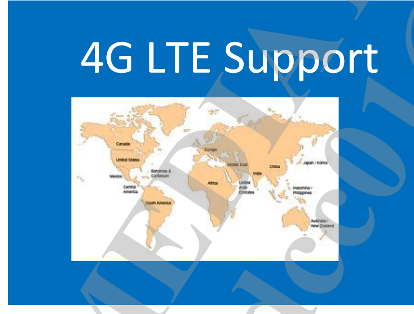
Brief Introduction to MT6737

- MT6737 is a new-generation LTE smart phone solution provided by MediaTek, which is produced on TSMC 28nm process with Octa-Core ARM Cortex-A53 running up to 1.25GHz.







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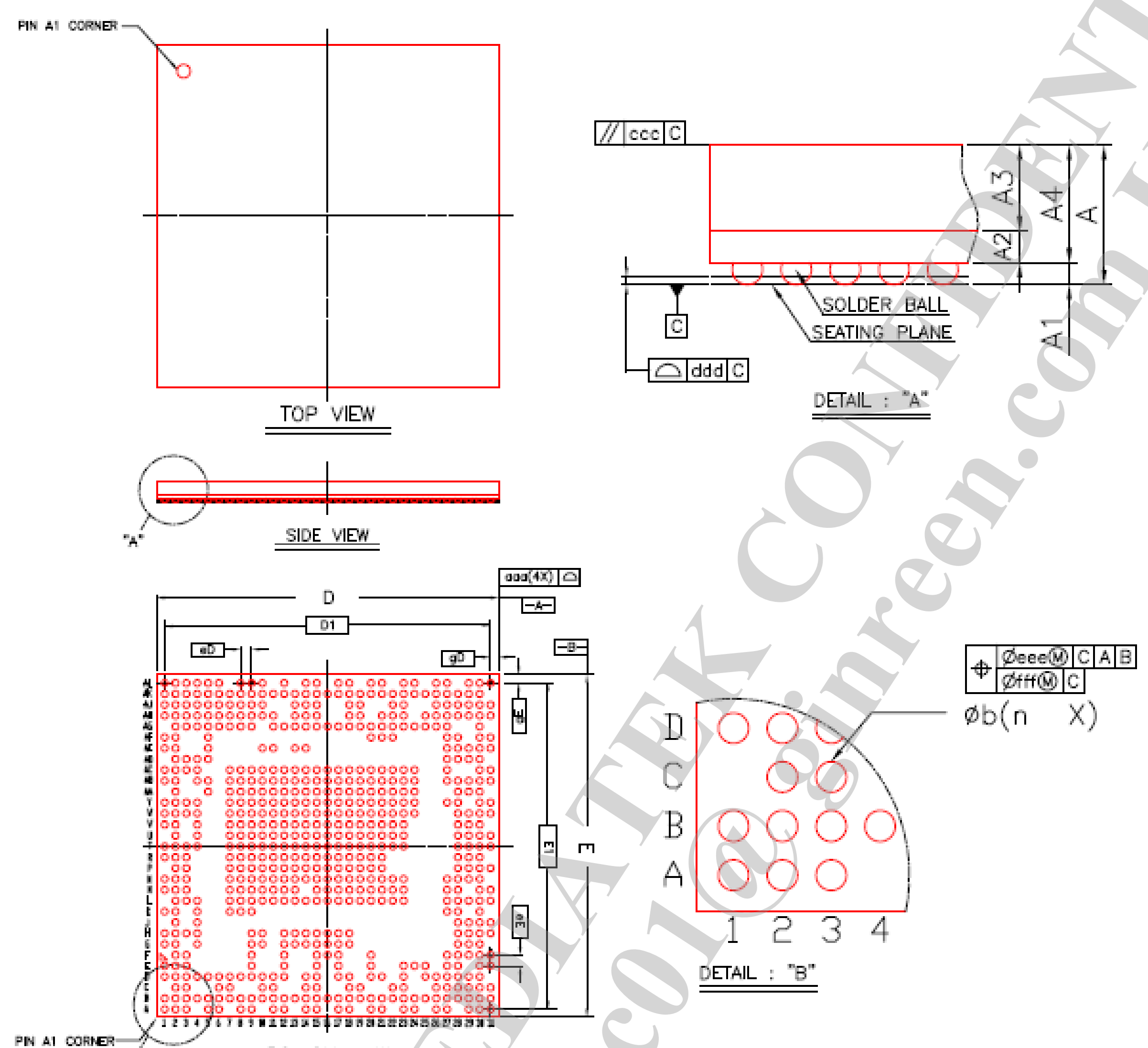
Package Outline of MT6737



Item		Symbol	Common Dimensions		
			MIN.	NOM.	MAX.
Package Type			MFC VFBGA		
Body Size	X	D	12.5	12.6	12.7
	Y	E	12.5	12.6	12.7
Ball Pitch	X	eD	0.40		
	Y	eE	0.40		
Mold Thickness		A3	0.45 Ref.		
Substrate Thickness		A2	0.15 Ref.		
Substrate+Mold Thickness		A4	0.55	0.60	0.65
Total Thickness		A	–	–	0.9
Ball Diameter			0.25		
Ball Stand Off		A1	0.12	0.16	0.20
Ball Width		b	0.20	0.25	0.30
Package Edge Tolerance		aaa	0.05		
Mold Flatness		ccc	0.10		
Coplanarity		ddd	0.08		
Ball Offset (Package)		eee	0.15		
Ball Offset (Ball)		fff	0.05		
Ball Count		n	641		
Edge Ball Center to Center	X	D1	12.00		
	Y	E1	12.00		
Edge Ball Center to Package Edge	X	gD	0.30		
	Y	gE	0.30		

- **Package info.**
  - **Body size: 12.6x12.6x0.9mm**
  - **Ball pitch: 0.4mm**
  - **Ball diameter: 0.25mm**
  - **Ball count: 641**

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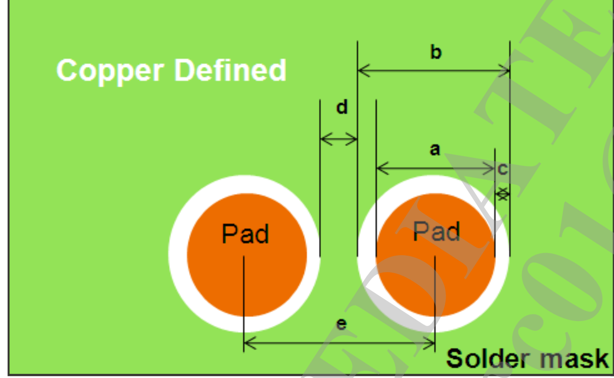
MT6737 Footprint Recommendation

Note:

- All MT6737 pins are recommended to use **copper defined** (as Figure 1)
- Recommended stencil opening ➔ 0.25mm square with 0.075R angle (as Figure 2 green area.)
- **We recommend you use 0.1/0.25mm (drill/land) laser via on PAD to improve the yield of SMT.**

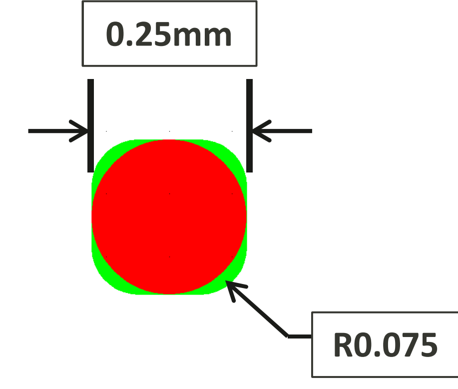
As Figure 1, all pins are recommended to use **copper defined.**
Pad size: 0.25mm; solder mask: 0.325mm

Figure 1



Copper Defined PCB land pad and Solder mask opening rule			
Land pad size	a	0.25mm	9.8mil
Solder mask opening	b	a+0.075mm	a+3mil
Solder mask clearance	c	0.038mm	1.5mil
Solder dam	d	0.075mm	3mil
Ball pitch	e	0.4mm	15.8mil

Figure 2



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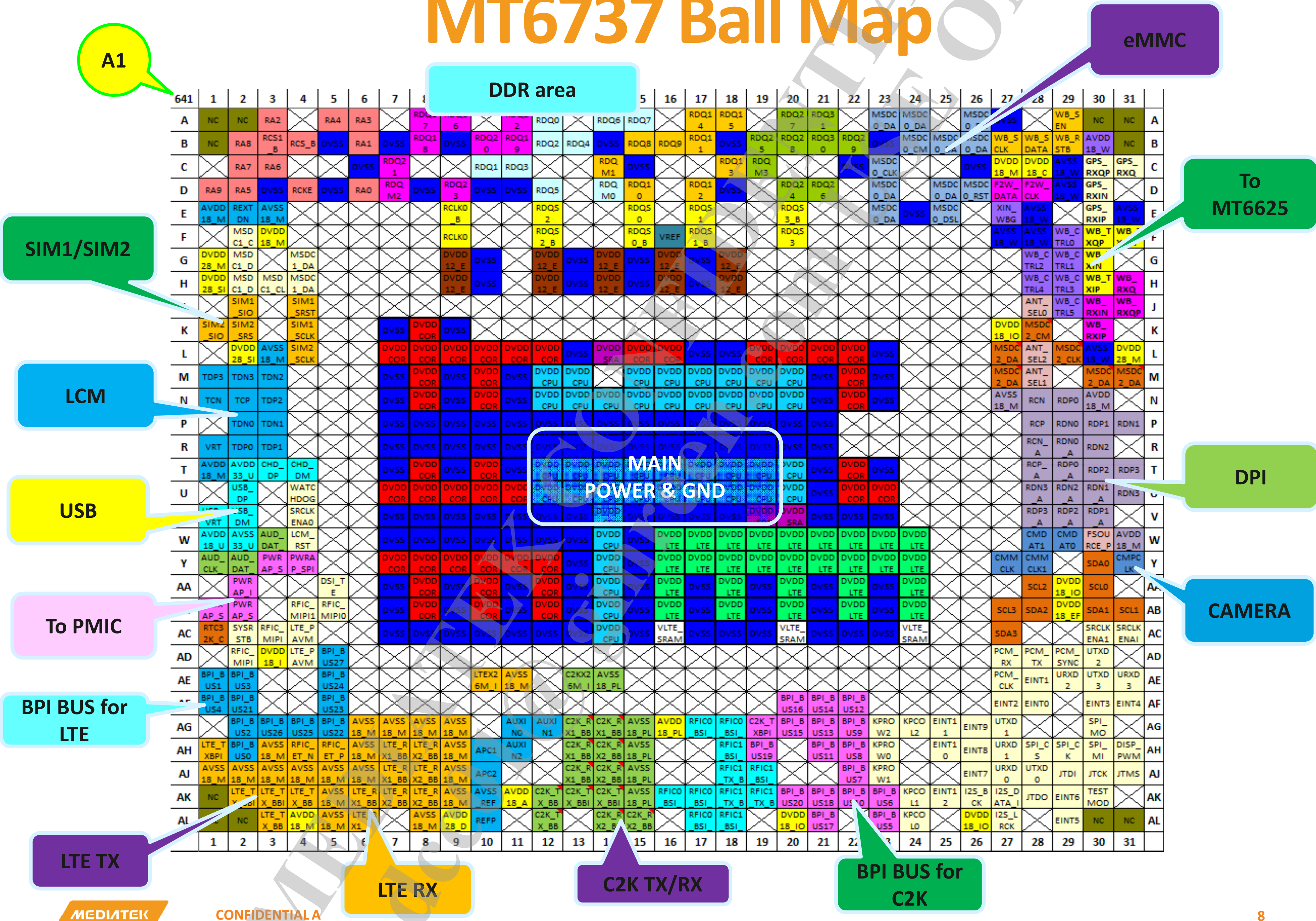
MT6737 Ball Map



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MT6737 PCB Stack-up Recommendations

- The total thickness of PCB is recommended to be less than 0.9mm±10%.
- Follow the recommended layer stack-up which defines the thickness and material to achieve optimal electrical performance.
- There are only specific arrangements on LPDDR2/3 and PDN (CPU, GPU, VCORE and LTE).
- For other signals, follow the PCB design guidelines in this document.
- Recommendations on stack-up:
  - 6 layers with HDI1
  - 8 layers with HDI1
  - 8 layers with HDI2 (stacked via)

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PCB Stack-up: 6 Layers with HDI1

6L HDI-1 (1-4-1), 0.8mm

Layers	Stackup	Suggestion (0.8 mm)				Layer definition Signal/Power/Ground (S/P/G)			
		Theoretic thickness (mm)	Theoretic thickness (mils)	Material	ER	LPDDR2/3	CPU	GPU/TOP/LTE	Others
SR		0.010	0.4	SR	3.5				
L1		0.033	1.3	Copper		G/S			S
		0.076	3.0	Prepreg (1080)	3.9				
L2		0.030	1.2	Copper		G/S			S
		0.102	4	Prepreg (2116)	4.1				
L3		0.015	0.6	Copper		G	G	G	G
		0.305	12.0	Core	4.4				
L4		0.015	0.6	Copper		G/S		P	G/P/S
		0.102	4.0	Prepreg (2116)	4.1				
L5		0.030	1.2	Copper		P	P		G/P/S
		0.076	3.0	Prepreg (1080)	3.9				
L6		0.033	1.3	Copper		G	G	G	G
SR		0.010	0.4	SR	3.5				
	Total	0.8 mm ±10%							

- **If you need to change the thickness of PCB, keep the PP thickness and adjust the core thickness to meet the requirement.**

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PCB Stack-up: 8 Layers with HDI1

8L HDI-1 (1-6-1), 0.8mm

Layers	Stackup	Suggestion (0.8 mm)				Layer definition Signal/Power/Ground (S/P/G)			
		Theoretic thickness (mm)	Theoretic thickness (mils)	Material	ER	LPDDR2/3	CPU	GPU/TOP/LTE	Others
SR		0.010	0.4	SR	3.5				
L1		0.033	1.3	Copper		G/S			S
		0.076	3.0	Prepreg (1080)	3.9				
L2		0.030	1.2	Copper		G/S			S
		0.076	3.0	Prepreg (1080)	3.9				
L3		0.015	0.6	Copper		G	G	G	G
		0.102	4.0	Core	4.1				
L4		0.015	0.6	Copper		G/S		P	G/P/S
		0.102	4.0	Prepreg (2116)	4.1				
L5		0.015	0.6	Copper		P	G	G	G/P/S
		0.102	4.0	Core	4.1				
L6		0.015	0.6	Copper		G	P		P/G
		0.076	3.0	Prepreg (1080)	3.9				
L7		0.030	1.2	Coper		G	G		G/S
		0.076	3.0	Prepreg (1080)	3.9				
L8		0.033	1.3	Copper		G	G	G	G/S
SR		0.010	0.4	SR	3.5				
	Total	0.8 mm ±10%							

- If you need to change the thickness of PCB, keep the PP thickness and adjust the core thickness to meet the requirement.

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PCB Stack-up: 8 Layers with HDI2 (Stagger via)

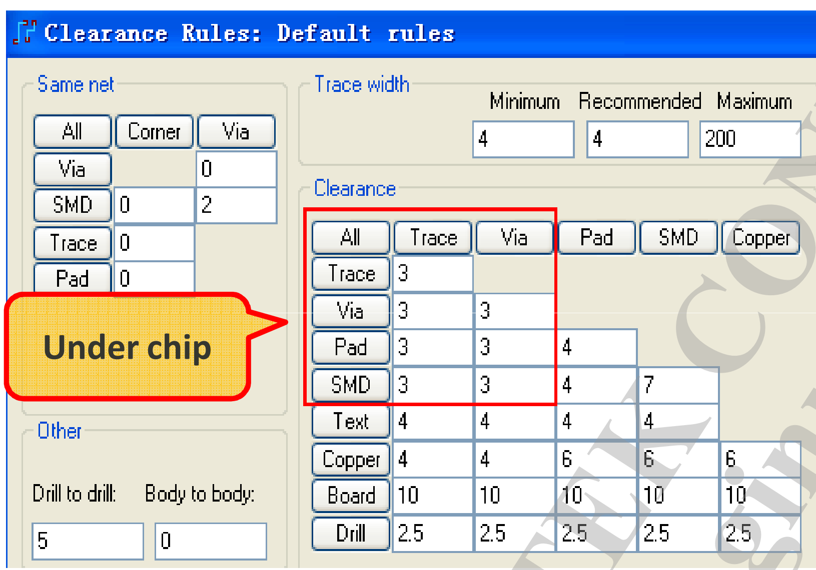
8L HDI-2 (1-1-4-1-1), 0.9mm/0.65mm

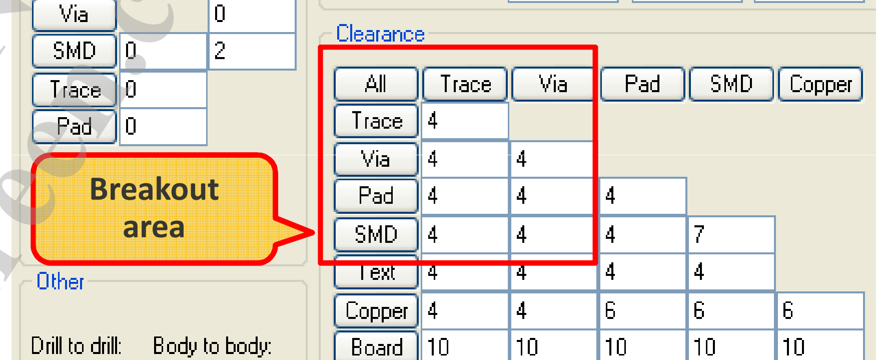
Layers	Stackup	Suggestion (0.9 mm)				Suggestion (0.65 mm)				Layout definition Signal/Power/Ground (S/P/G)			
		Theoretic thickness (mm)	Theoretic thickness (mils)	Material	ER	Theoretic thickness (mm)	Theoretic thickness (mils)	Material	ER	LPDDR2 /3	CPU	GPU/ TOP/LTE	Others
SR		0.010	0.4	SR	3.5	0.010	0.4	SR	3.5				
L1		0.033	1.3	Copper		0.033	1.3	Copper		G/S			S
		0.076	3.0	Prepreg (1080)	3.9	0.056	2.2	Prepreg (1080)	3.9				
L2		0.030	1.2	Copper		0.030	1.2	Copper		G/S			S
		0.076	3.0	Prepreg (1080)	3.9	0.056	2.2	Prepreg (1080)	3.9				
L3		0.031	1.2	Copper		0.030	1.2	Copper		G	G	G	G
		0.102	4.0	Prepreg (2116)	4.1	0.056	2.2	Prepreg (1080)	3.9				
L4		0.014	0.6	Copper		0.014	0.6	Copper		G/S		P	G/P/S
		0.178	7.0	Core	4.3	0.102	4.0	Core	4.1				
L5		0.014	0.6	Copper		0.014	0.6	Copper		P		G	G/P/S
		0.102	4.0	Prepreg (2116)	4.1	0.056	2.2	Prepreg (1080)	3.9				
L6		0.031	1.2	Copper		0.031	1.2	Copper		G	P		P/G
		0.076	3.0	Prepreg (1080)	3.9	0.056	2.2	Prepreg (1080)	3.9				
L7		0.030	1.2	Coper		0.030	1.2	Coper		G	G		G/S
		0.076	3.0	Prepreg (1080)	3.9	0.056	2.2	Prepreg (1080)	3.9				
L8		0.033	1.3	Copper		0.033	1.3	Copper		G	G	G	G/S
SR		0.010	0.4	SR	3.5	0.010	0.4	SR	3.5				
	Total	0.9 mm ±10%				0.65 mm ±10%							

- **If you need to change the thickness of PCB, keep the PP thickness and adjust the core thickness to meet the requirement.**

Common Rules and Via Type

- **Min. trace width/spacing:**
  - **Under MT6737: 3/3mil**
  - **Breakout area: 4/4 mil**





- Via type:
  - Blind Via (under chip) ➔ 4/10 mil
  - Blind Via (outside chip) ➔ 4/12 mil
  - Buried Via ➔ 10/18mil
  - Through Via ➔ 12/20 mil

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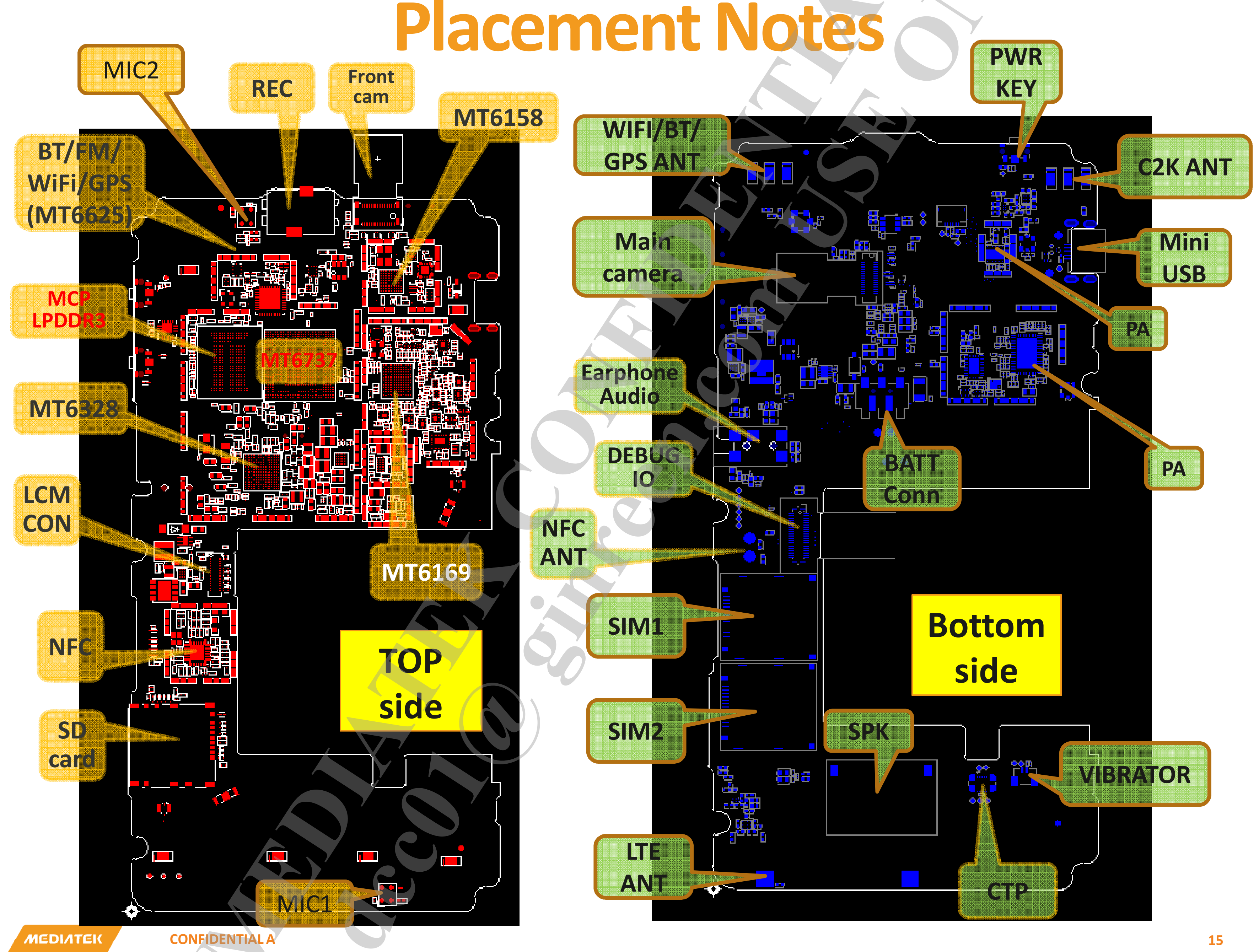
Placement Notes



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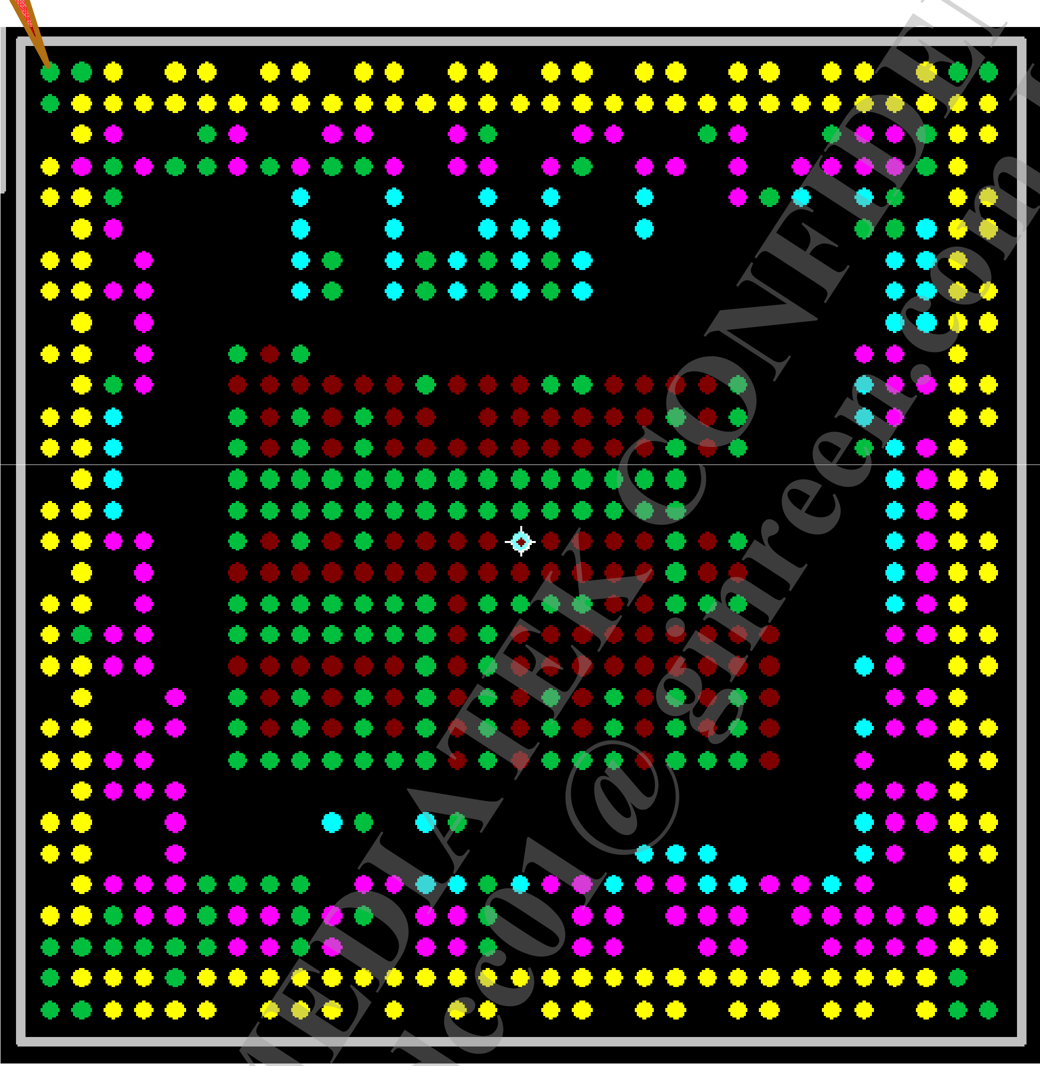
MT6737 Fan Out



Fan out by top layer for the 1st & 2nd rows (balls marked in yellow).

Fan out by layer2 for the 3rd to 5th rows. Place blind vias (4/10mil) on ball pads (balls marked in pink).

Fan out by layer4 for he 5th to ~rows (balls marked in blue). **When you place the buried via, keep GND and PWR plane as solid as possible.**

Green and red balls are all PWR/GND balls. **Keep GND and PWR plane as solid as possible.**

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PCB Module Design

- **You recommend you adopt modules by MediaTek as the first priority.**

  As the design trend turns to developing light, thin and higher battery capacity on smart phones, the complexity on system design becomes a great challenge nowadays. It is a time and cost consuming process to meet the layout constraints and deliver a good signal and power integrity.

  To assist our customers to rapidly design a correct, performance-oriented and reliable layout on PCB, we have introduced the **MMD (MediaTekModuleDesign)** solution. MMD provides optimized CPU and MCP layout design with guaranteed performance and stability. Meanwhile, it greatly shortens the time to market.

  The main purpose of MMD is providing a convenient and flexible solution for our customers. The ideal condition is to implant the modules without any modification. However, if the module cannot match your mechanics, you can still partially adopt MMD and enjoy the benefits from it.

  Contact your corresponding FAE when you have any problem in introducing MMD.

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Enabling your High-speed Digital Design~

SIE (SignalIntegrityExpress): SI/PI simulation support

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MT6737 Ball List for LPDDR3 Interface

Ball	#	Signal Name	Description	Grouping
C7, A8, B8, A9, D9, B10, C10, A11, B11, C11, A12, B12, D12, B13, A14, A15, B15, D15, B16, A17, B17, D17, A18, C18, B19, A20, B20, D20, A21, B21, D21, B22	32	**DQ[0:31]**	Data bus	**DQ**
D7, C14, D14, C19	4	**DQM[0:3]**	Data mask	
E12, F12, E15, F15, E17, F17, E20, F20	8	**DQS_T[0:3]** **DQS_C[0:3]**	Differential data strobe pair	**DQS**
D1, B2, C2, D2, A3, C3, A5, A6, B6, D6	10	**CA[0:9]**	Command/Address inputs	**C/A**
B3, B4, D4	3	**CKE** **CS0_N** **CS1_N**	Clock enable Chip select	
E2	1	**EXTDN**	Drive Strength Calibration	
F16	1	**VREF**	Reference voltage	
E9, F9	2	**CLK0_T** **CLK0_C**	Differential clock pair	**CLK**
G9, H9, G12, H12, G14, H14, G16, H16, G18, H18	8	**DDRV**	Provide LPDDR3 DRAM controller I/O power. V=1.2V, (1.14V/1.3V)	**LPDDR3_PWR**

The LPDDR3 memory interface operates up to 1600Mbps and will suffer signal integrity issues due to strong electromagnetic coupling between signal traces. Thus, we strongly recommend you adopt the MMD (MediaTek Module Design) solution. If MMD cannot be employed into your design, follow the PCB design guidelines given below.

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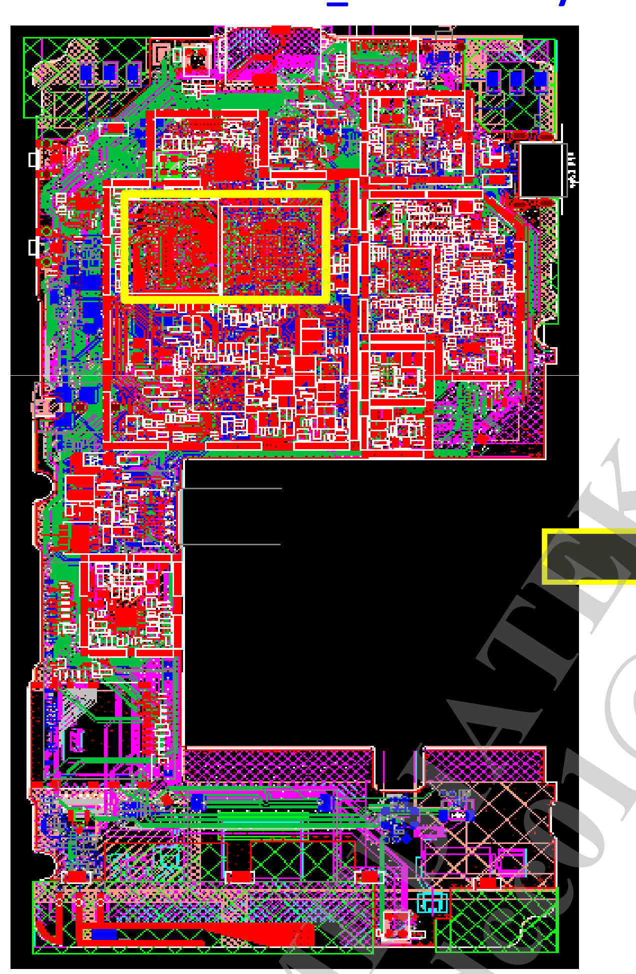
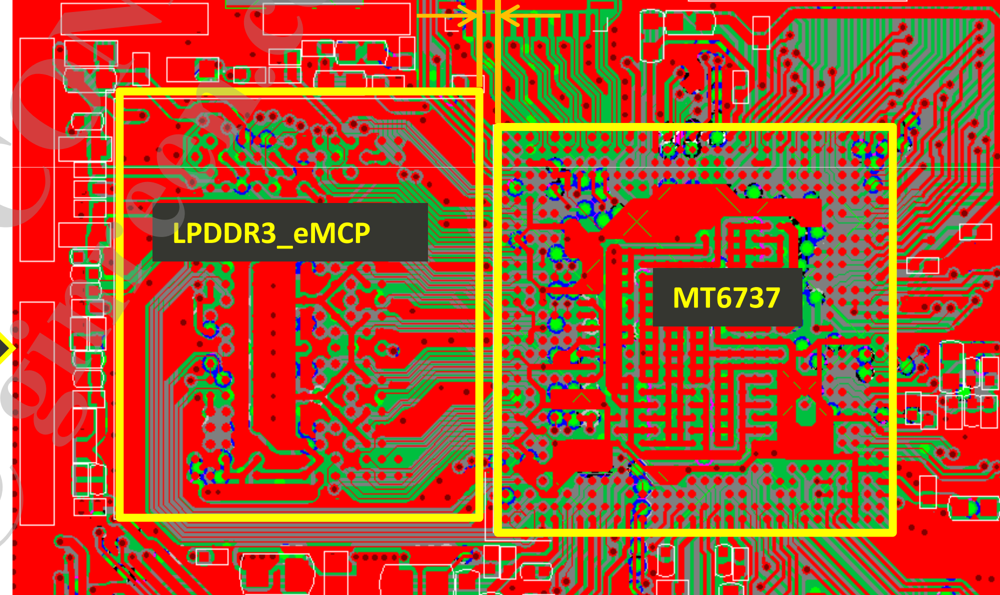
Placement Recommendation for LPDDR3_MCP

LPDDR3_eMCP placement guidelines:

1. Place LPDDR3_eMCP close to MT6737 and control △Y min.= 0.5mm (min. is better).
2. Place it as the figure below. If there is a location shift, route the traces between MT6737 and LPDDR3_MCP directly.





Top-Side

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PCB Design Guidelines for LPDDR3_1600Mbps

Basic constraint and layer suggestions

1. Follow the routing constraint and layer suggestion as the figure below and route the traces between MT6737 and LPDDR3_eMCP as short as possible.
2. Trace width/spacing:
   Under MT6737: 3mil/3mil
   Outside MT6737: 3mil/3mil
3. Route at L1, L2 and L4. Keep L3 as solid GND plane and L5 as solid PWR plane.
4. Do not overlap the signal traces between L1 and L2.
5. All the signal traces don't need length control and impedance control.

∆Y min. =0.5mm

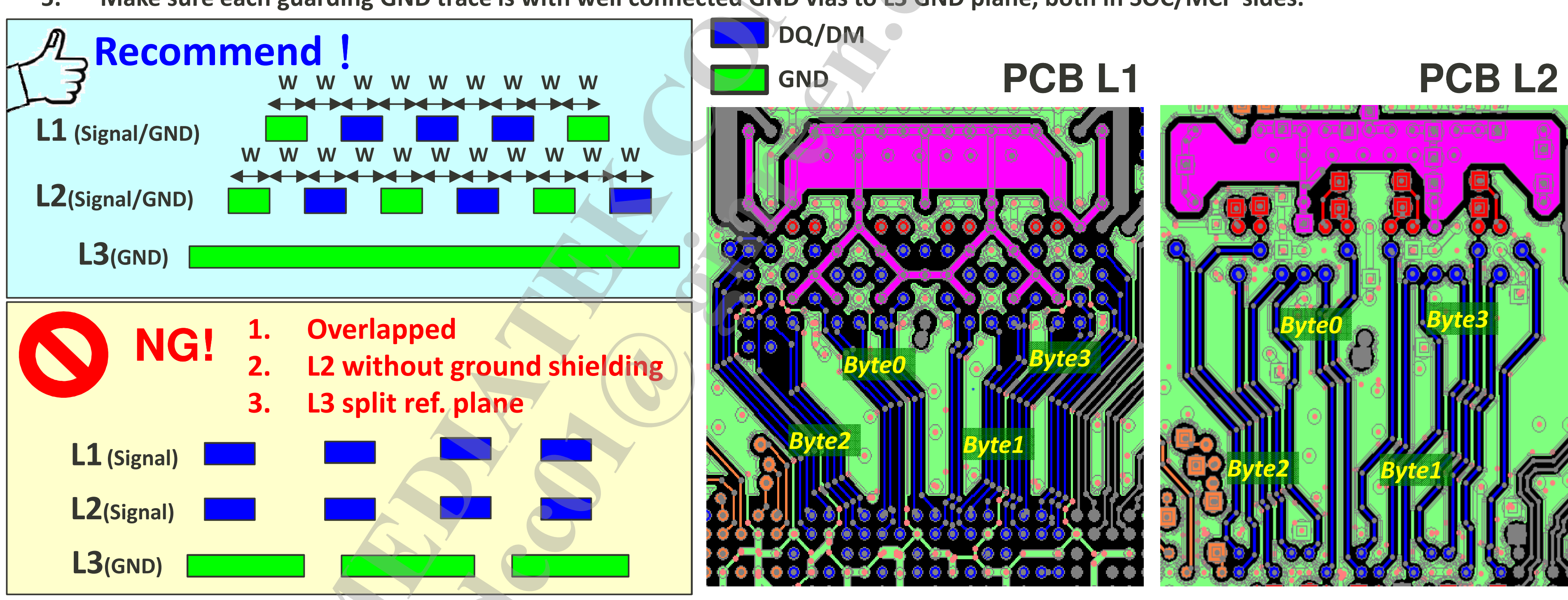
LPDDR3_eMCP

MT6737

PCB Design Guidelines for DQ

Ball	#	Signal Name	Description	Grouping
C7, A8, B8, A9, D9, B10, C10, A11, B11, C11, A12, B12, D12, B13, A14, A15, B15, D15, B16, A17, B17, D17, A18, C18, B19, A20, B20, D20, A21, B21, D21, B22	32	**RDQ[0:31]**	Data bus	**DQ**
D7, C14, D14, C19	4	**RDQM[0:3]**	Data mask	

1. **Route signal at L1 and L2. Keep L3 as a solid ground plane. Keep DQ&DM as short as possible.**
2. **Except for the breakout region, keep the ground trace at L2 under signal traces at L1.**
3. **Isolate every three signal traces with 3mil/3mil ground traces at L1 (as the figure below).**
4. **Isolate each signal trace with 3mil/3mil ground traces at L2. Do not overlap the signal traces between L1 and L2 (as the figure below).**
5. **Make sure each guarding GND trace is with well connected GND vias to L3 GND plane, both in SOC/MCP sides.**



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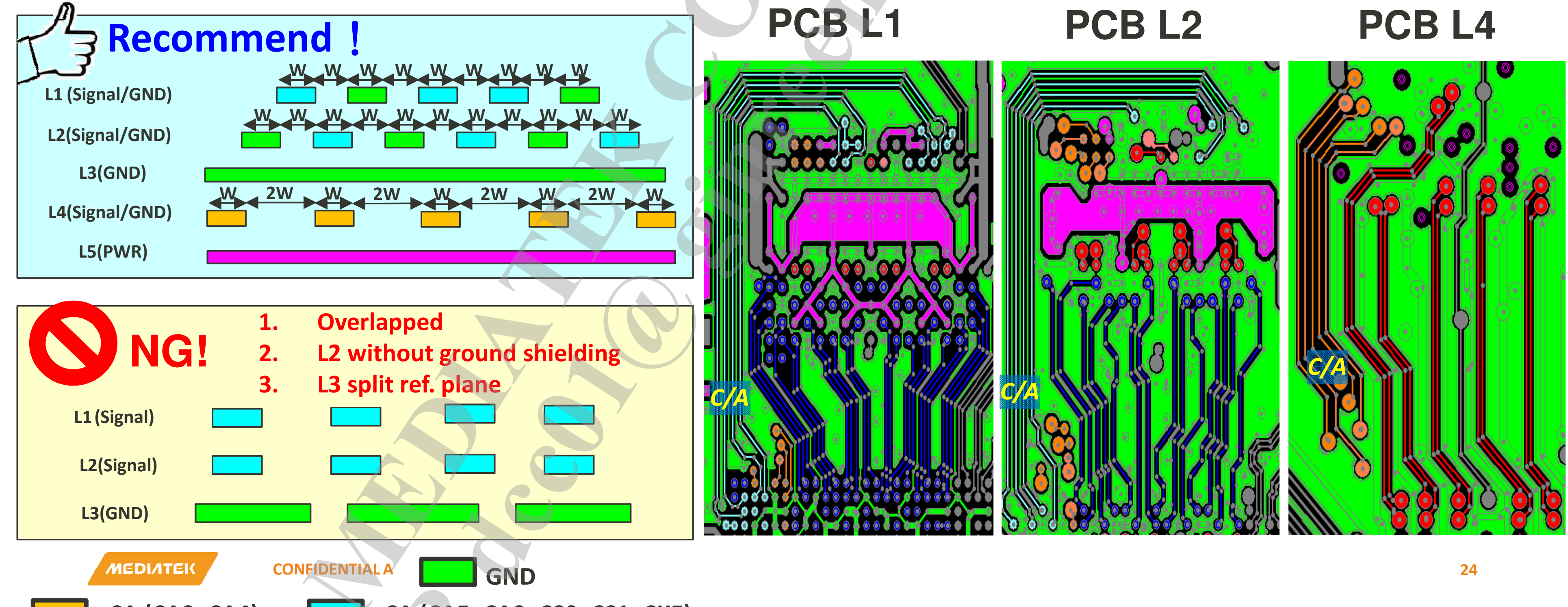
PCB Design Guidelines for CA

Ball	#	Signal Name	Description	Grouping
D1, B2, C2, D2, A3, C3, A5, A6, B6, D6	10	**RA[0:9]**	Command/Address inputs	**C/A**
B3, B4, D4	3	**RCKE/RCS0_B** **RCS1_B**	Clock enable Chip select	

1. **Route CA5~CA9, CKE,CS0,CS1 at L1/L2. Keep solid planes at L3. Keep trace length as short as possible.**
2. **Route CA0~CA4,at L4. Keep space 2W.**
3. **Route DQ/DM/CMD/CA(CA5~CA9, CS0, CS1, CKE) at L1 & L2.**
   1) **Isolate every signal trace with 3mil/3mil ground traces at L1.**
   2) **Isolate every signal trace with 3mil/3mil ground traces at L2.**
   3) **Do not overlap the signal traces between L1 and L2 (as the figure below).**



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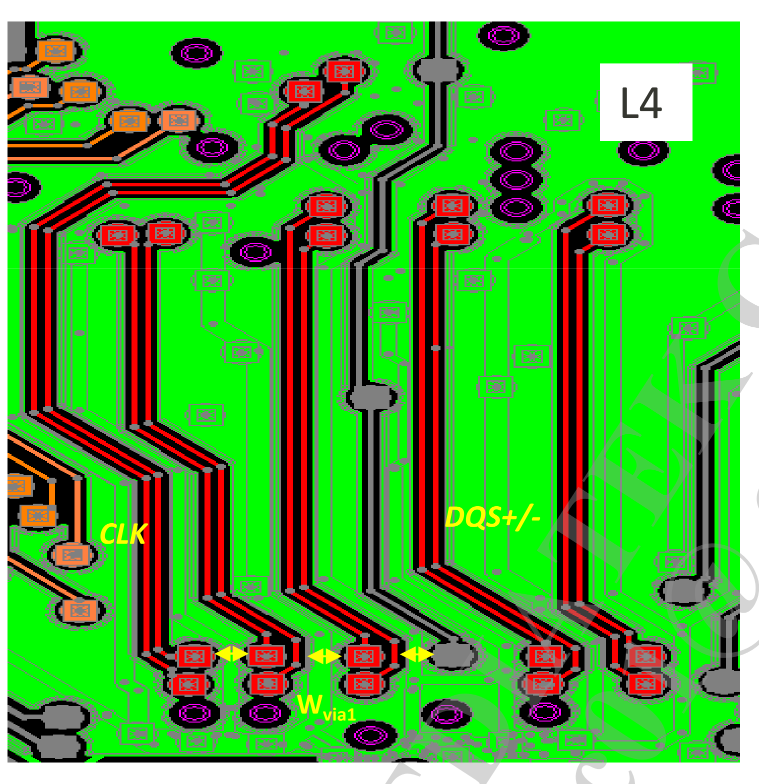
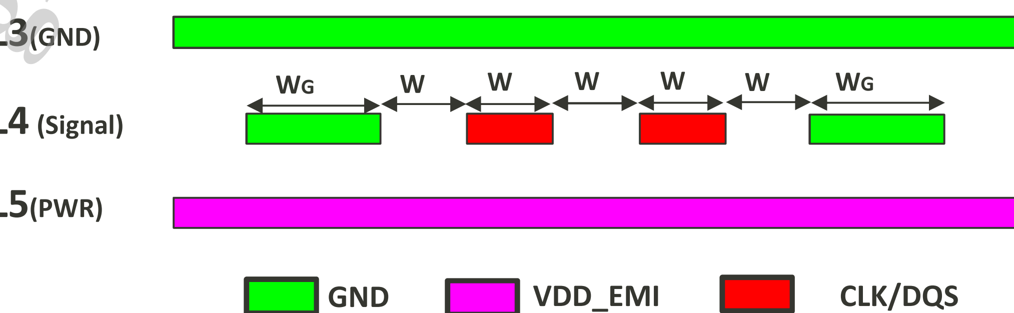
PCB Design Guidelines for DQS, CLK

Ball	#	Signal Name	Description
E12, F12, E15, F15, E17, F17, E20, F20	8	**EDQS[0:3] /EDQS[0:3]**	Differential data strobe pair **(DQS)**
E9, F9	2	**EDCLK /EDCLK**	Differential clock pair **(CLK)**



PCB layout guidelines:

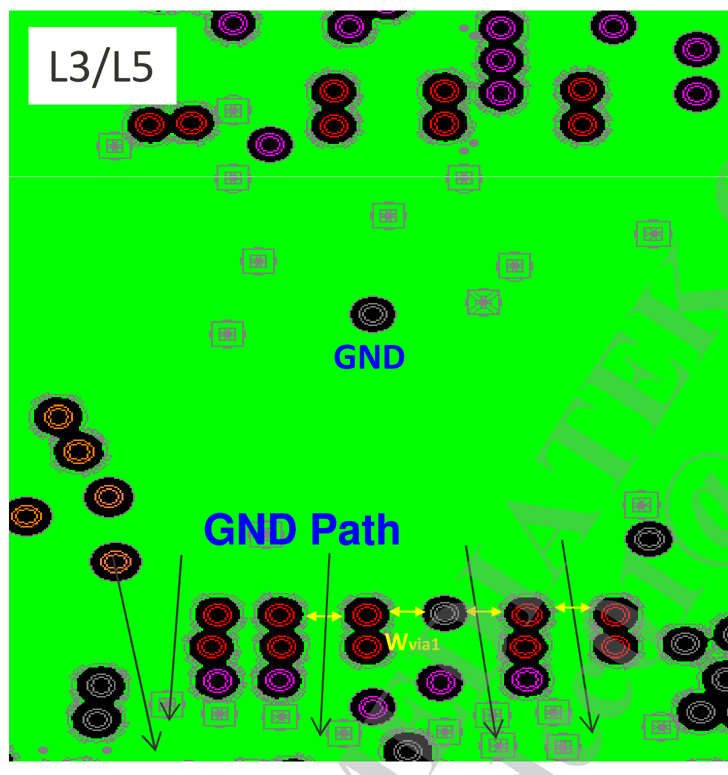
1. **DQS and CLK are differential pairs**
   Keep P/N parallel route at L4. Keep solid planes at L3 and L5.
   Isolate each differential pair with 3mil/3mil ground traces
2. **Trace width / spacing:**
   Under MT6737: 3mil/3mil
   Outside MT6737: 3mil/3mil
   $W_G \geqq$ 3mil
3. **Keep via spacing, $W_{via1} \geq$ 10 mil, to form power and ground passages.**

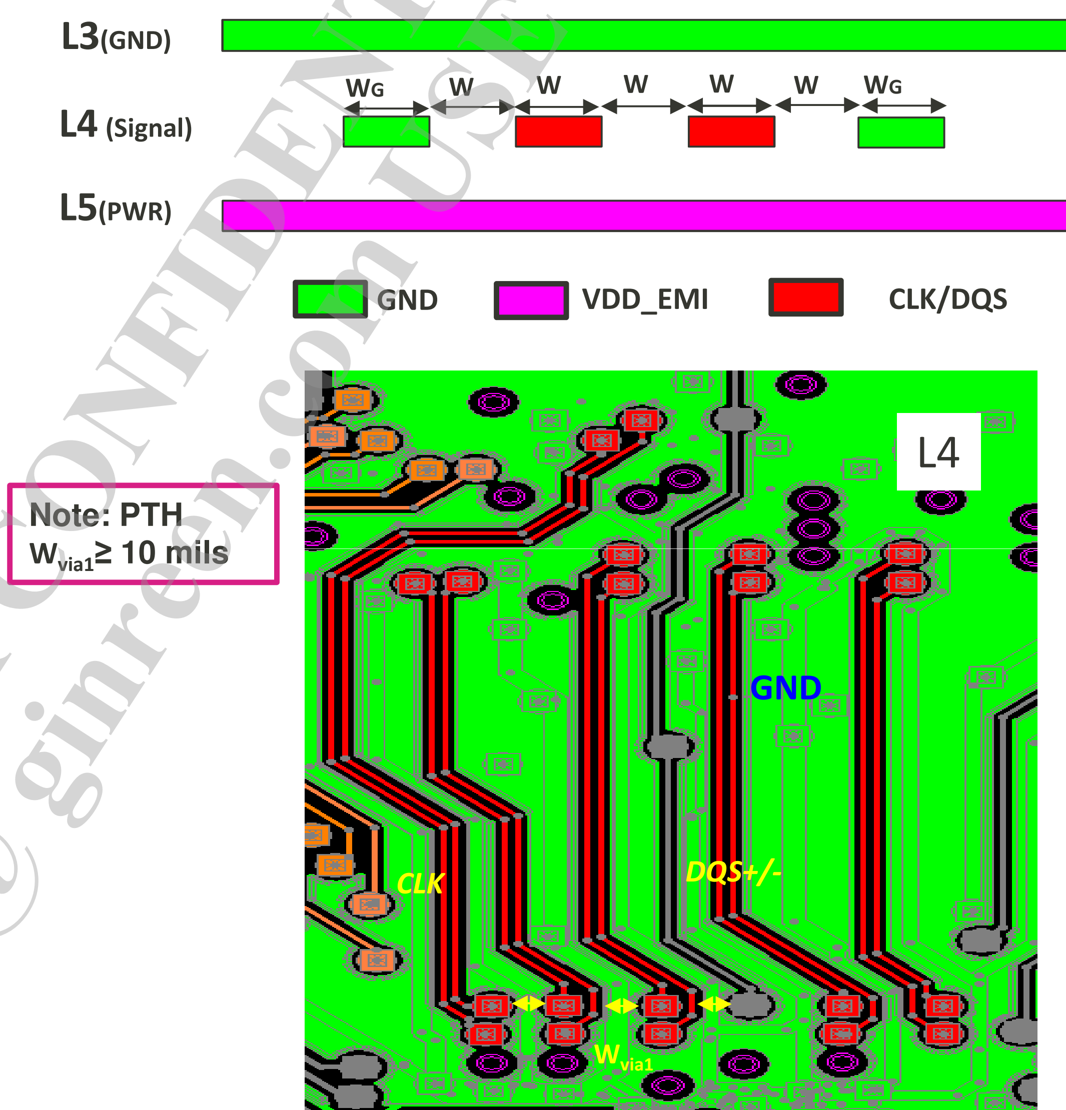


Guidelines for PWR/GND Plane

PCB layout guidelines:

1. Prevent voids by vias. Keep solid planes at L3 and L5.
2. Keep all the traces within L3 (GND) and **L5(PWR) boundaries**.
3. Keep via spacing, $W_{via2} \geq$ 10 mil, to form power and ground passages.





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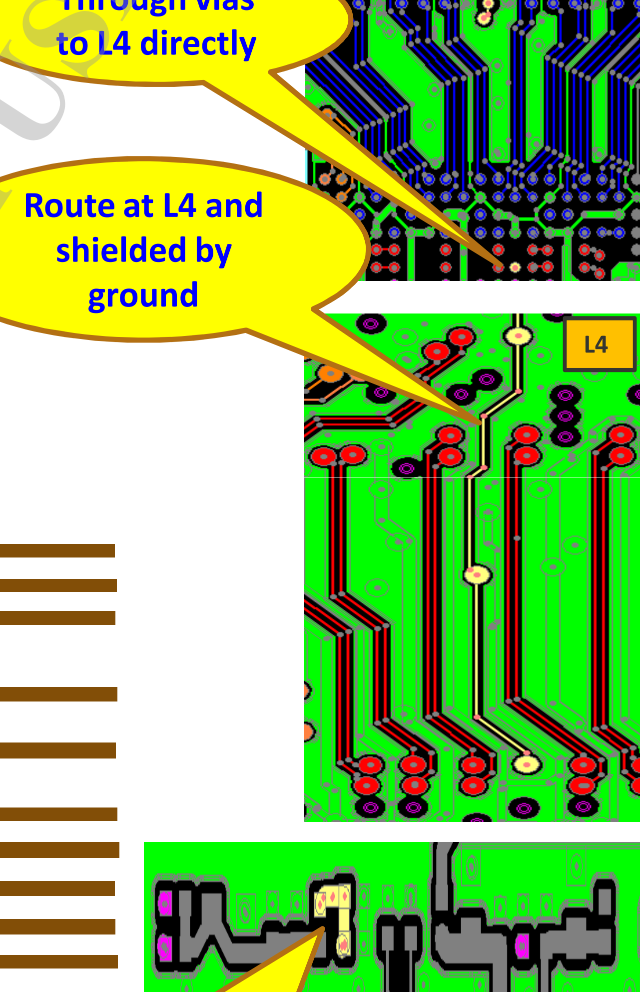
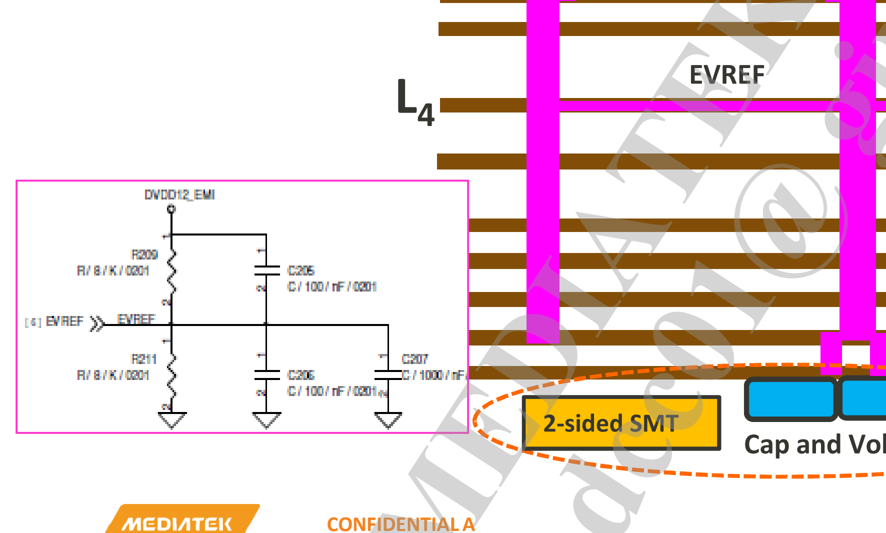
LPDDR3 VREF Guideline

Ball	#	Signal Name	Description
F16	1	VREF	Reference Voltage

1. Place voltage divider consisting of two **1K~10K Ω ±1% resistors.**
2. Do not route close to other high-speed signal traces.
3. Isolate EVREF with ground or power.
4. Route directly to L4 with ground isolation as the figure below. Keep 4mil spacing with ground at L4.
5. Place two 0.1uF and one 1uF decoupling capacitors in the bottom layer.





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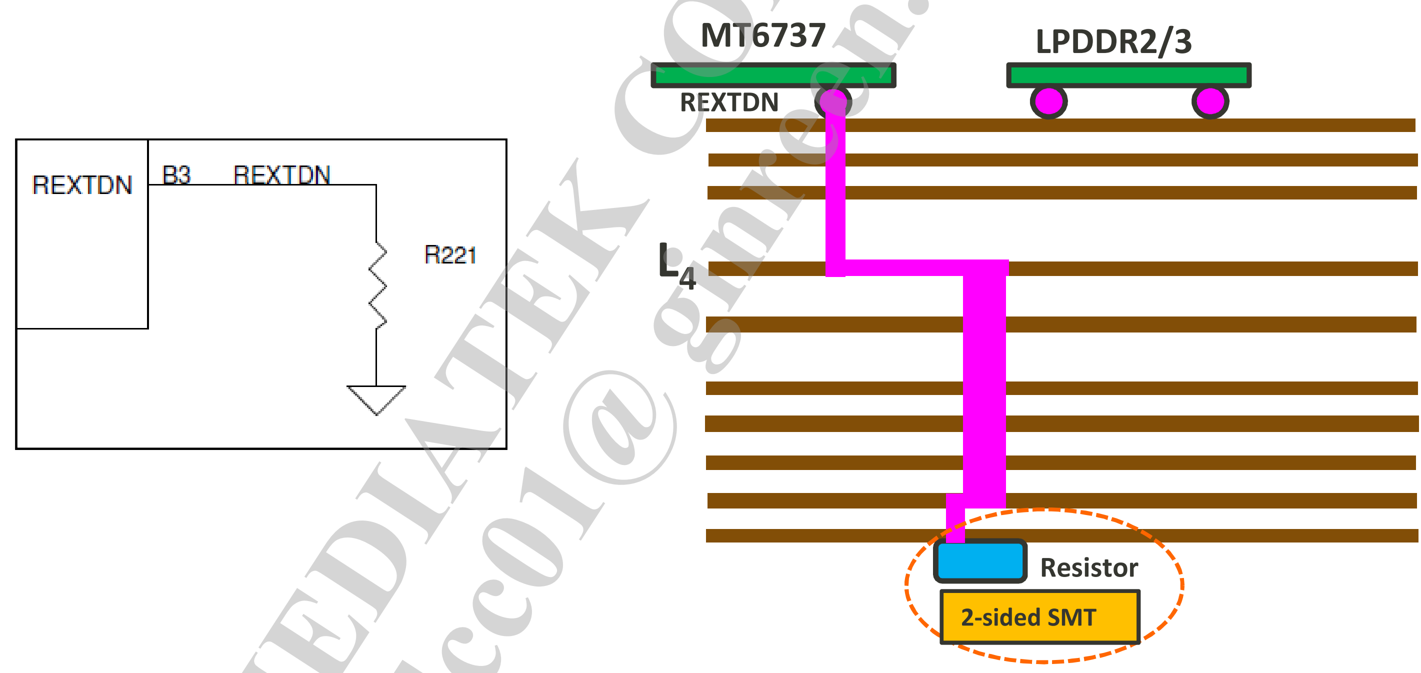
LPDDR3 REXTDN Guideline

Ball	#	Signal Name	Description
E2	1	**REXTDN**	**Drive Strength Calibration**

1. **Place one 36Ω (1%) pull-down resistor for REXTDN. (Default not SMT)**
2. **Route directly to L4 with ground isolation as the figure below.**



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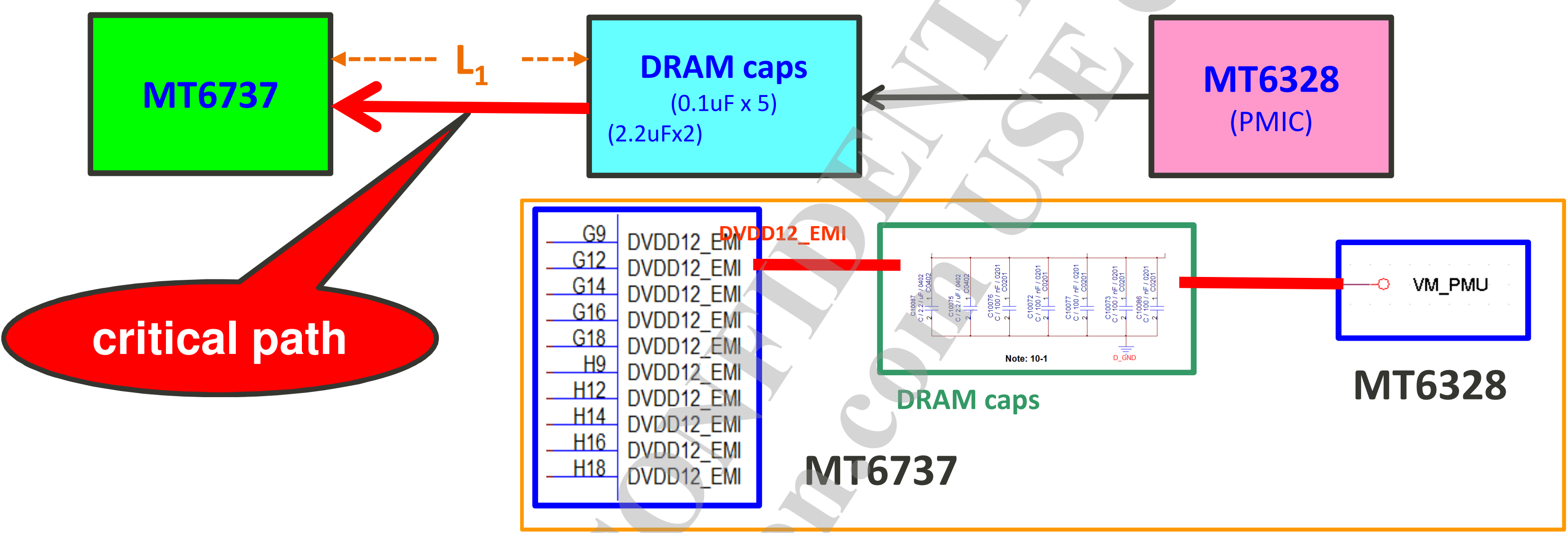
PCB Layout Guidelines for DVDD12_EMI



1. The PDN networks start from MT6328(PMIC) output pin, pass through DRAM caps and finally to MT6737.
2. The "critical pass" is defined as the path from DRAM caps to MT6737. The routing should meet the design guideline.
3. Place five 0.1uF and two 2.2uF capacitors close to MT6737 DVDD12_EMI.
4. L1 is defined as the trace length from DRAM caps to MT6737 DVDD12_EMI. It should be routed as short as possible. Other PCB design guidelines are listed below.

   2-sided SMT: Place five 0.1uF and two 2.2uF caps right under the ball-outs of MT6737 DVDD12_EMI with moderate amount of direct vias. Please strictly follow the design constraints.

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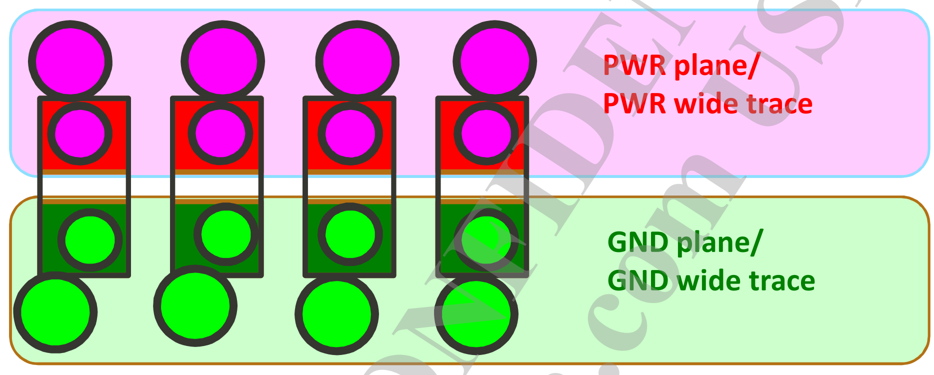
Via Interconnection for DVDD12_EMI



- **Design suggestions for via interconnection**

Via interconnect is critical in delivering current between each layer and is usually the bottleneck in the entire PDN networking. Thus, we strongly recommend you follow the related PWR/GND layout guidelines.

1. **PWR/GND via is recommended to connect to the "wide power trace" and also placed as close as possible to the decoupling capacitor.**
2. **Each decoupling capacitor should have at last one pair PWR/GND via. If the routing space is available, more PWR/GND vias are recommended. The ratio of Pad: Laser via: PTH via =1: 1: 1. Try to distribute PTH & Laser vias uniformly.**

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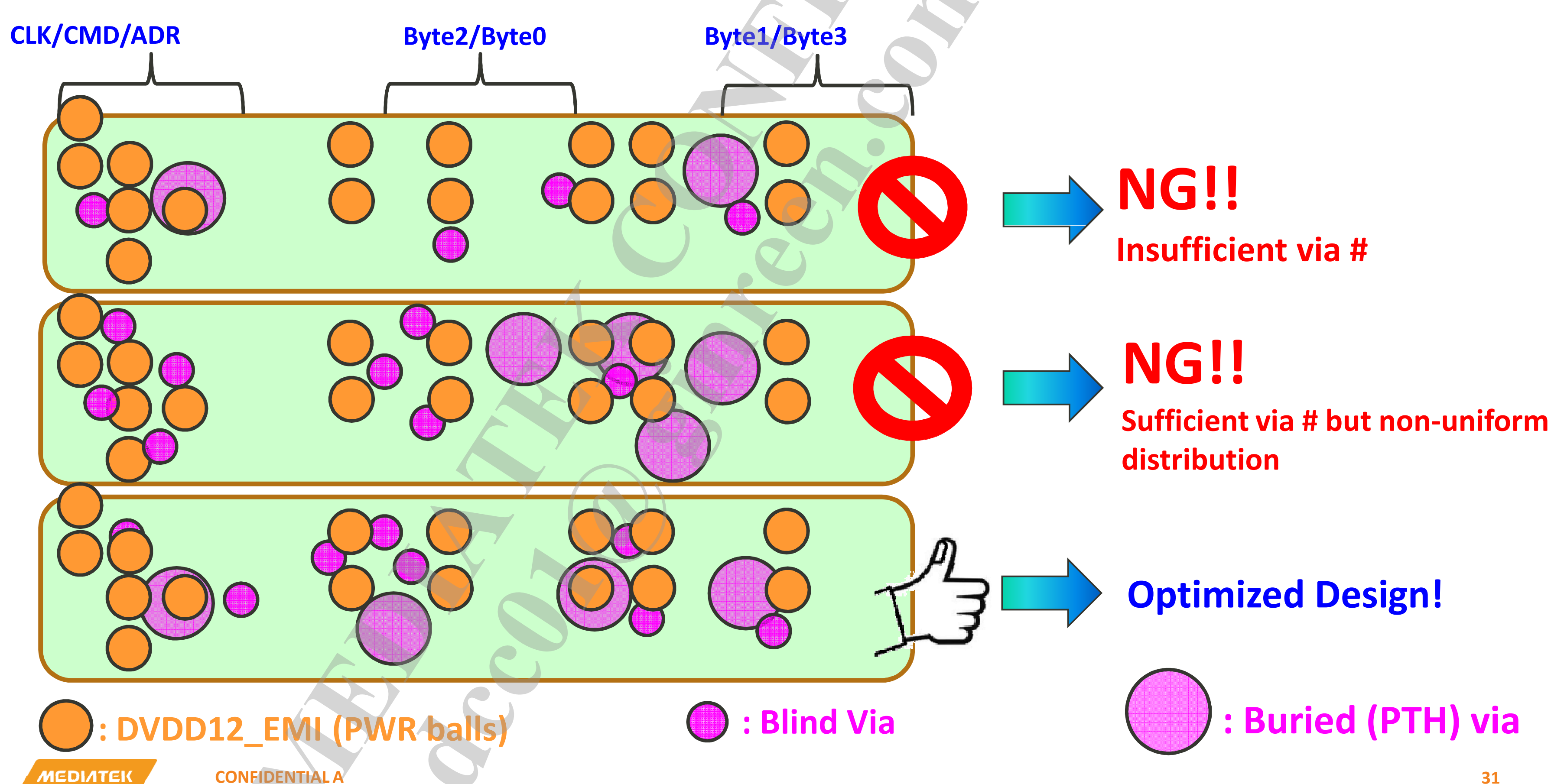
Via Interconnection for DVDD12_EMI

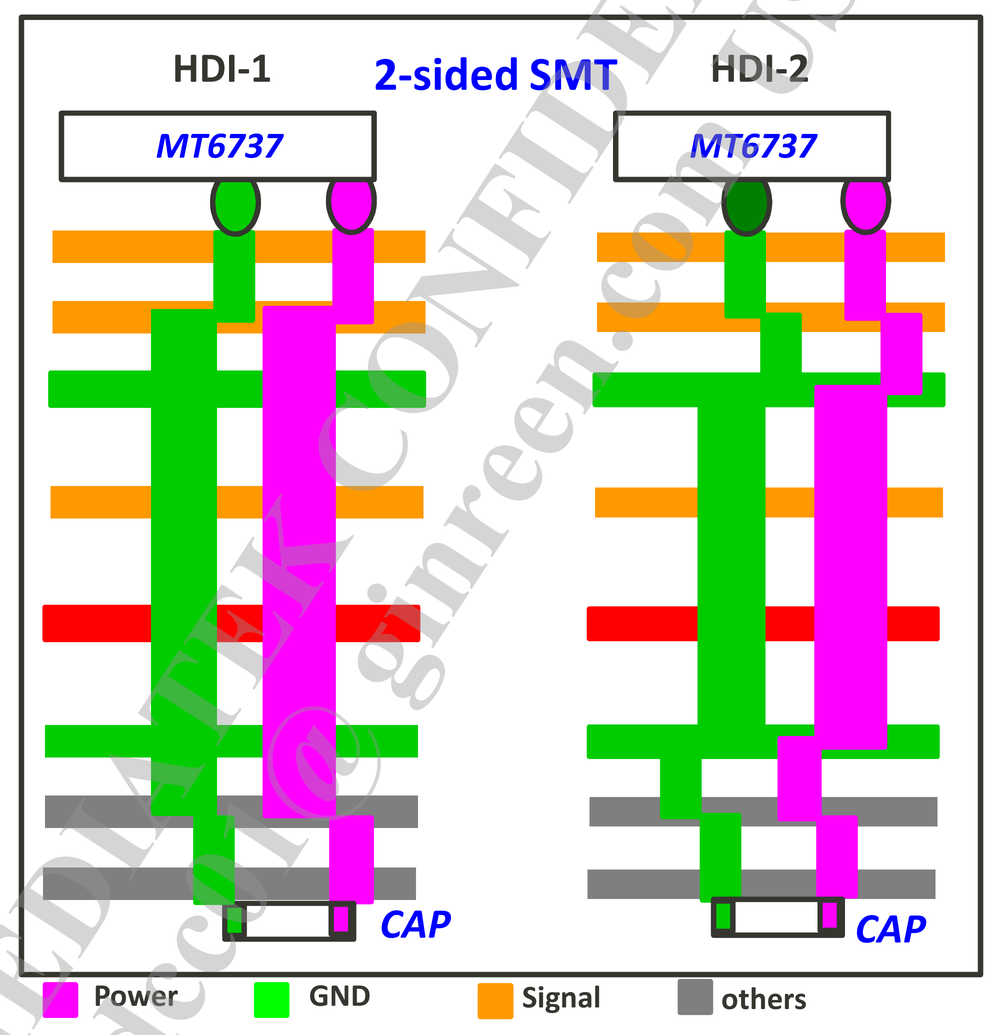
- **PCB Via Interconnection Suggestions for DVDD12_EMI:** (Top view of MT6737 PCB)

1. The # of blind via & PTH via beneath the DVDD12_EMI region should meet the requirement. Taking MT6737 for example, the minimum requirement is 5 blind vias & 5 PTH vias.
2. More blind vias are recommended (>5). Use the "via on ball" process " on DVDD12_EMI ball" and directly connect it to the wide power trace and PTH via. In addition, make sure the blind vias & PTH vias are uniformly distributed.
3. Both PWR and GNR are critical in reducing PDN inductance. Place PWR PTHs as close as possible to GND PTHs.



Via Interconnection for DVDD12_EMI

1. Place GND vias as close as possible to PWD vias to reduce PWR/GND inductance.
2. The ratio of "# of GND via: # of PWR via" is recommended 1:1.



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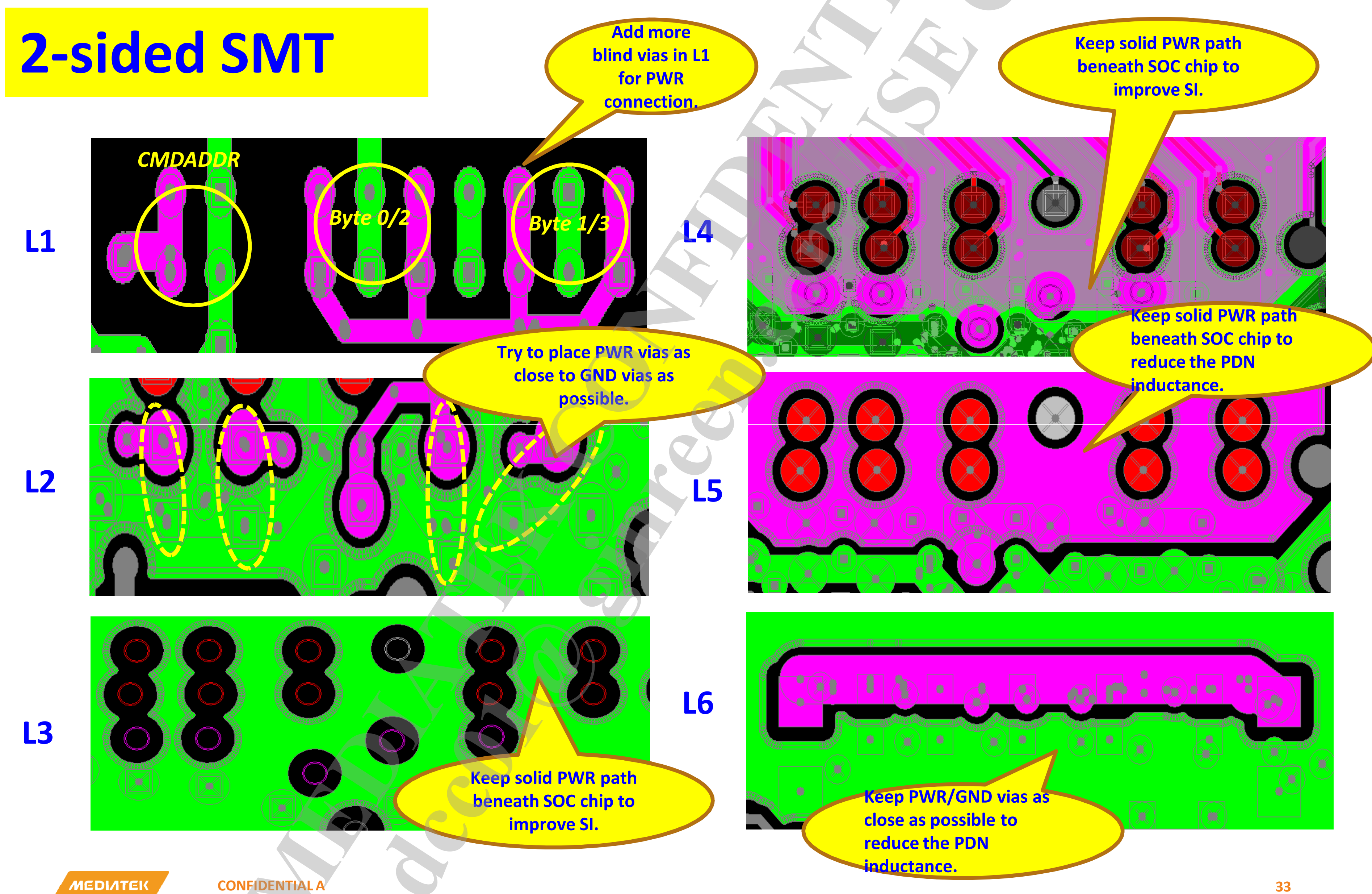
Via Interconnection for DVDD12_EMI Design Example



Outlines

- **Brief Introduction to MT6737**
- **Packaging**
  - Package Outline of MT6737
  - MT6737 Footprint Recommendation
  - MT6737 Ball Out Design
- **General Guidelines**
  - PCB Stack-up Recommendation
  - Common Rules and Via Type
  - Placement Notes
  - MT6737 Fan Out
- **Design Guidelines for High-Speed Digital Signals**
  - LPDDR3
  - LPDDR2
  - PDN Design
- **Others**
  - MT6737 RF Interface - MT6169 - MT6158
  - MT6328 (PMU)
  - MT6625 (BT/FM/WiFi/GPS)
  - USB/MIPI/SIM Card/T-Card/eMMC/Differential Pair Layout Suggestion

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MT6737 Ball List for LPDDR2 Interface

Ball	#	Signal Name	Description	Grouping
C7, A8, B8, A9, D9, B10, C10, A11, B11, C11, A12, B12, D12, B13, A14, A15, B15, D15, B16, A17, B17, D17, A18, C18, B19, A20, B20, D20, A21, B21, D21, B22	32	**DQ[0:31]**	Data bus	**DQ**
D7, C14, D14, C19	4	**DQM[0:3]**	Data mask	
E12, F12, E15, F15, E17, F17, E20, F20	8	**DQS_T[0:3]** **DQS_C[0:3]**	Differential data strobe pair	**DQS**
D1, B2, C2, D2, A3, C3, A5, A6, B6, D6	10	**CA[0:9]**	Command/Address inputs	**C/A**
B3, B4, D4	3	**CKE** **CS0_N** **CS1_N**	Clock enable Chip select	
E2	1	**EXTDN**	Drive Strength Calibration	
F16	1	**VREF**	Reference voltage	
E9, F9	2	**CLK0_T** **CLK0_C**	Differential clock pair	**CLK**
G9, H9, G12, H12, G14, H14, G16, H16, G18, H18	8	**DDRV**	Provide LPDDR2 DRAM controller I/O power. V=1.2V, (1.14V/1.3V)	**LPDDR2_PWR**

The LPDDR2 memory interface operates up to 1066Mbps and will suffer signal integrity issues due to strong electromagnetic coupling between signal traces. Thus, we strongly recommend you adopt the MMD (MediaTek Module Design) solution. If MMD cannot be employed into your design, follow the PCB design guidelines given below.

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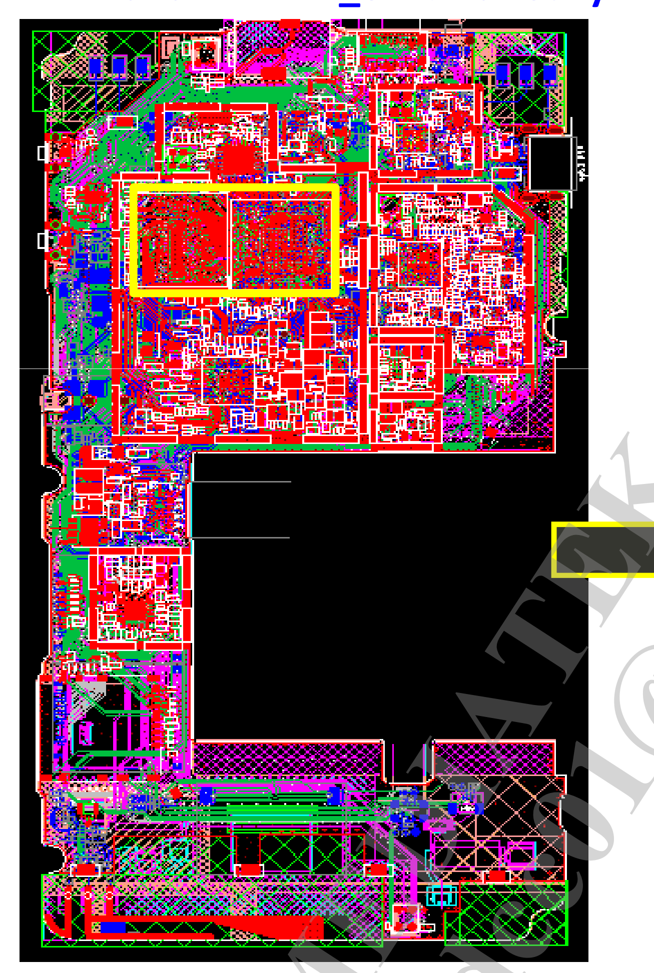
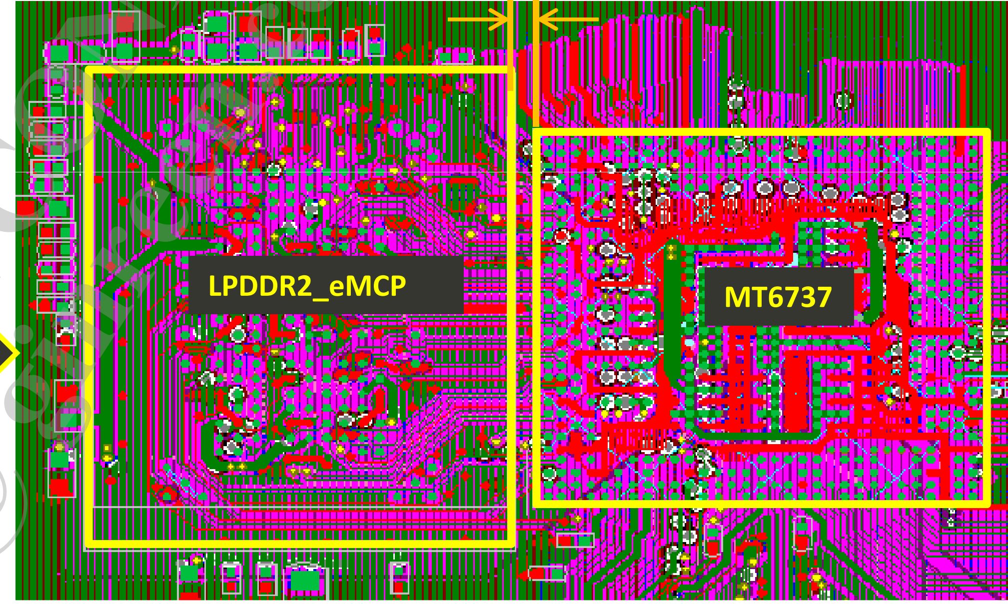
Placement Recommendation for LPDDR2_eMCP

LPDDR2_eMCP placement guidelines:

1. Place LPDDR2_eMCP close to MT6737 and control **△Y min.= 1mm (min. is better).**
2. Place as the figure below. If there is a location shift, **route the traces between MT6737 and LPDDR2_eMCP directly.**





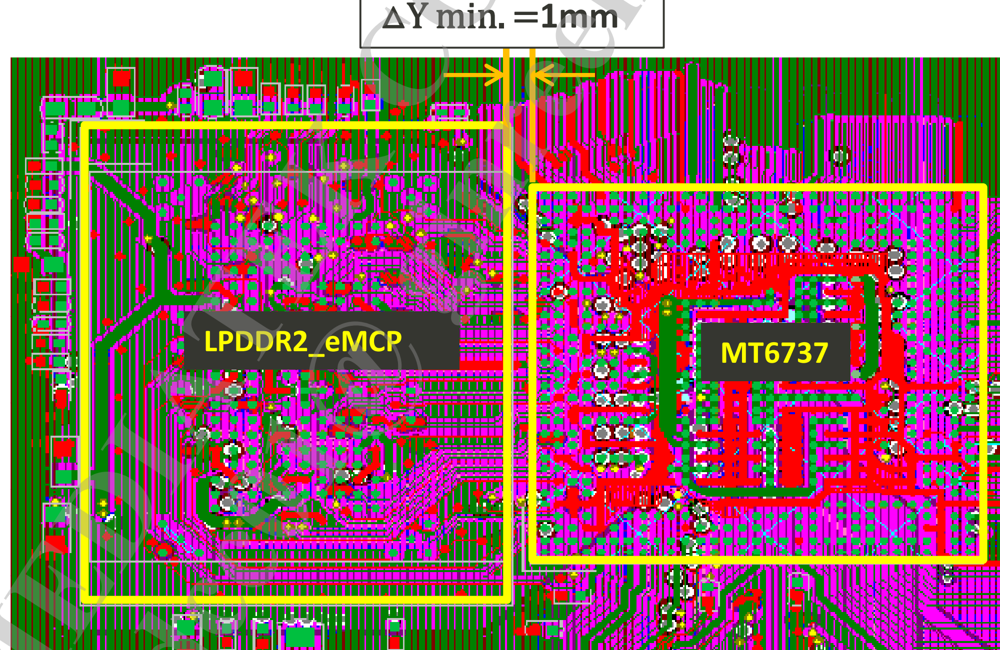
Top-Side

MEDIATEK CONFIDENTIAL A

PCB Design Guidelines for LPDDR2_1066Mbps

Basic constraint and layer suggestion

1. Follow the routing constraint and layer suggestion as the figure below and route the traces between MT6737 and LPDDR2_eMCP as short as possible.
2. Trace width/spacing:
   Under MT6737: 3mil/3mil
   Outside MT6737: 3mil/3mil
3. Route at L1, L2, and L4. Keep L3 as solid GND plane and L5 as solid PWR plane.
4. Do not overlap the signal traces between L1 and L2.
5. All the signal traces don't need length control and impedance control.
6. The routing rule is identical to LPDDR3.



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Outlines

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  - MT6625 (BT/FM/WiFi/GPS)
  - USB/MIPI/SIM Card/T-Card/eMMC/Differential Pair Layout Suggestion

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Basic Concept of PDN

- With the increasing demand on switching current and power consumption, the conventional PCB design concept is no longer sufficient in dealing with GHz level CPU for the current high-end smart phones. Thus, a well-designed PDN (Power Delivery Network) on PCB is greatly significant, especially in the high-performance octa-core MT6737.
- The whole PDN should include all the interconnections & current return path from PMIC to MT6737. The performance mainly depends on the location & number of power traces, PWR/GND vias and decoupling capacitors. These parameters are defined in the following guidelines.

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Ball List Table

MT6737 ball list for VPROC & VCORE:

Ball	#	Signal Name	Description
M12, M13, M15, M16, M17, M18, M19, M20, N12, N13, N14, N15, N16, N17, N18, N19, N20, T12, T13, T14, T15, T16, T17, T18, T19, T20, U12, U13, U14, U15, U16, U17, U18, U19, U20, V14, W14, Y14, AA14, AB14, AC14	41	VPROC	Provides application processor CPU. V=1.25V Maximum current 5A
K8, L7, L8, L9, L10, L11, L12, L15, L16, L19, L20, L21, L22, M8, M10, M22, N8, N10, N22, T8, T10, T22, U7, U8, U9, U10, U11, U22, U23, Y7, Y8, Y9, Y10, Y11, Y12, AA8, AA10, AA12, AB8, AB10, AB12	41	VCORE	Provides application processor core power. V=1.15V Maximum current 3.2A
W16, W17, W18, W19, W20, W21, W22, W23, W24, Y16, Y17, Y18, Y19, Y20, Y21, Y22, Y23, Y24, AA16, AA18, AA20, AA22, AA24, AB16, AB18, AB20, AB22, AB24	28	VLTE	Provides application processor core power. V=1.05V Maximum current 2A

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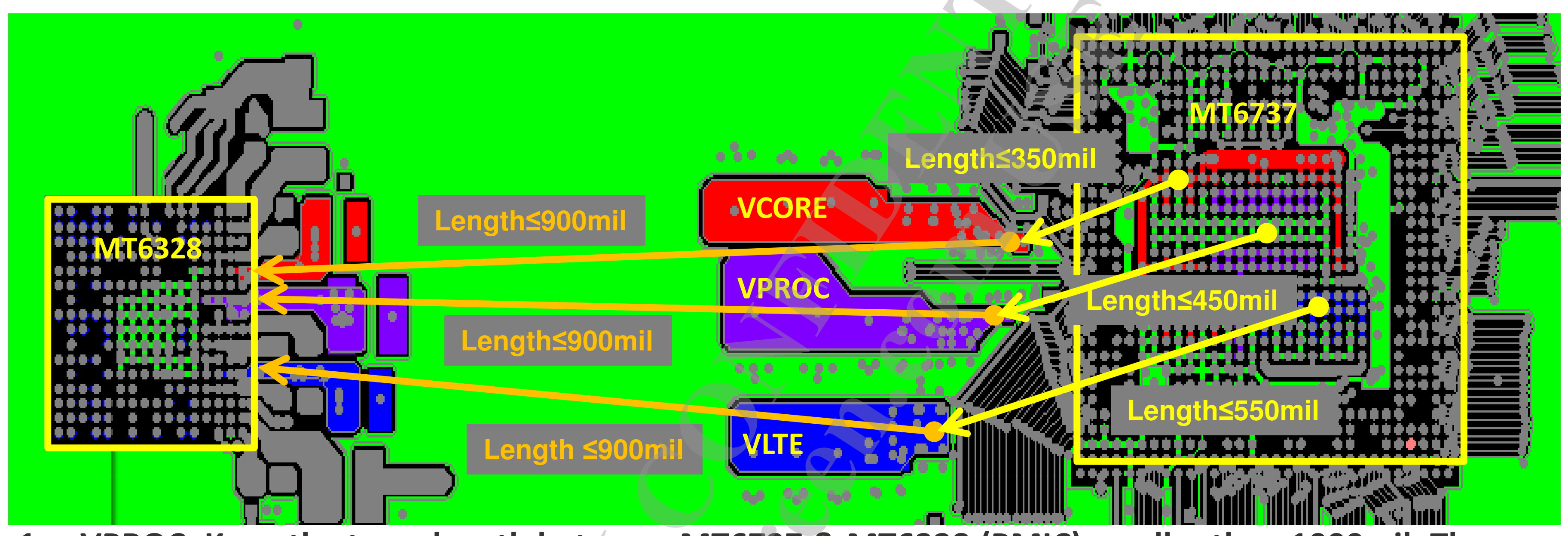
PMIC Placement Suggestions



1. VPROC: Keep the trace length between MT6737 & MT6328 (PMIC) smaller than 1000mil. The area from MT6737 to 1st-caps should be smaller than 450mil. The area from 1st-cap to MT6328 should be smaller than 900mil.
2. VCORE: Keep the trace length between MT6737 & MT6328 (PMIC) smaller than 1500mil. The area from MT6737 to 1st-caps should be smaller than 350mil. The area from 1st-cap to MT6328 should be smaller than 900mil.
3. VLTE: Keep the trace length between MT6737 & MT6328 (PMIC) smaller than 1000mil. The are from MT6737 to 1st-caps should be smaller than 550mil. The area from 1st-cap to MT6328 should smaller than 900mil.

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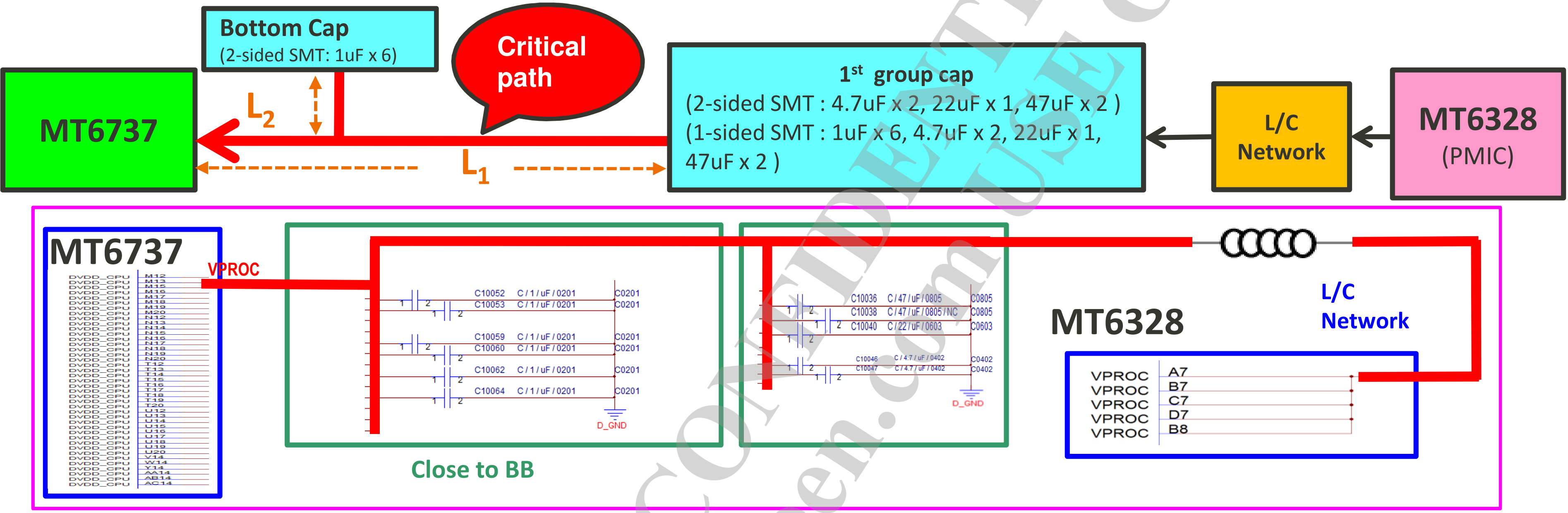
Guidelines for CPU Power: VPROC



1. The whole PDN (Power Distribution Network) is from MT6328 (PMIC) output pin, through first stage LC lowpass filter, to the 1st group cap. The PDN is the source of all the switching current.
2. The "Critical-Path" is defined as the power trace segment from the 1st group cap to MT6737 VPROC. The critical path design is strongly recommended to follow the given PCB layout guideline.
3. 2-sided SMT: Place six 1uF SMD capacitors as close to VPROC balls as possible. In the "1st group cap" region, place two 4.7uF, one 22uF and two 47uF SMD capacitors.
   1) L_1 is defined as the critical path from "1st group cap" to MT6737 VPROC. The corresponding PCB routing rules are given as the following:
      - PWR adopts 1 layer PWR, L_1 length≤ 450mil; L_1 width≥ 120mil. Total 1 layer PWR & 1 layer GND (suggestion 1).
   2) L_2 is defined as the power trace segment from "Bottom cap" to MT6737. The corresponding PCB routing rules are given as the following:
      - Place six 1uF SMD capacitors right beneath the MT6737 VPROC and connect the SMD capacitors to wide power trace directly. Try to make L_2 as short as possible.

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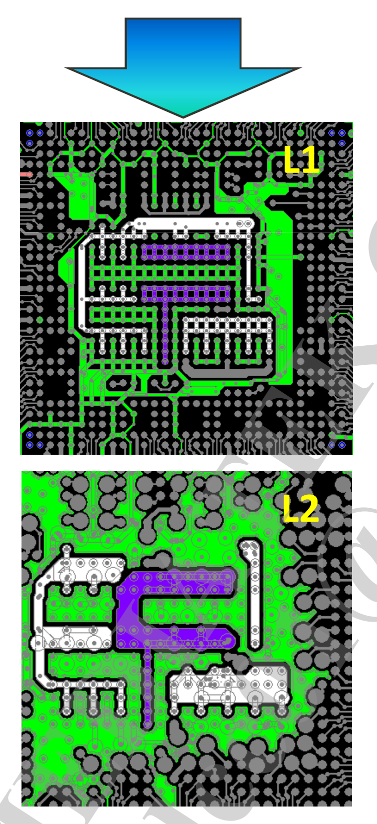
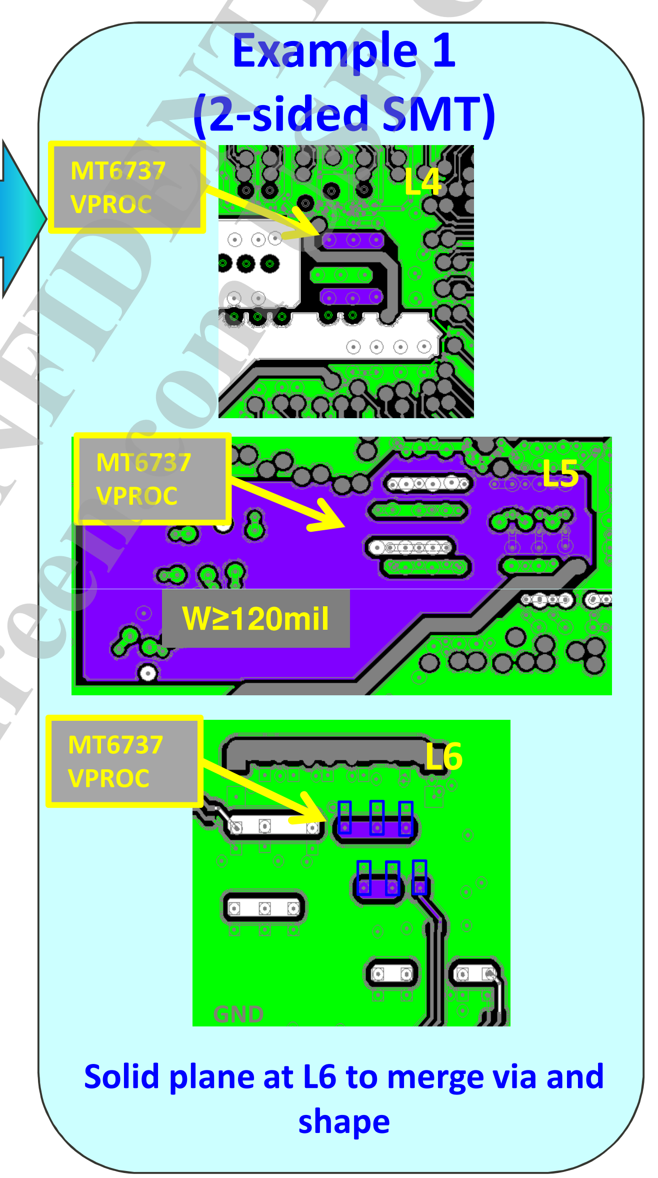
Guidelines for CPU Power: VPROC

Design examples & suggestions" for the wide power trace from 1st group cap" to MT6737 VPROC:





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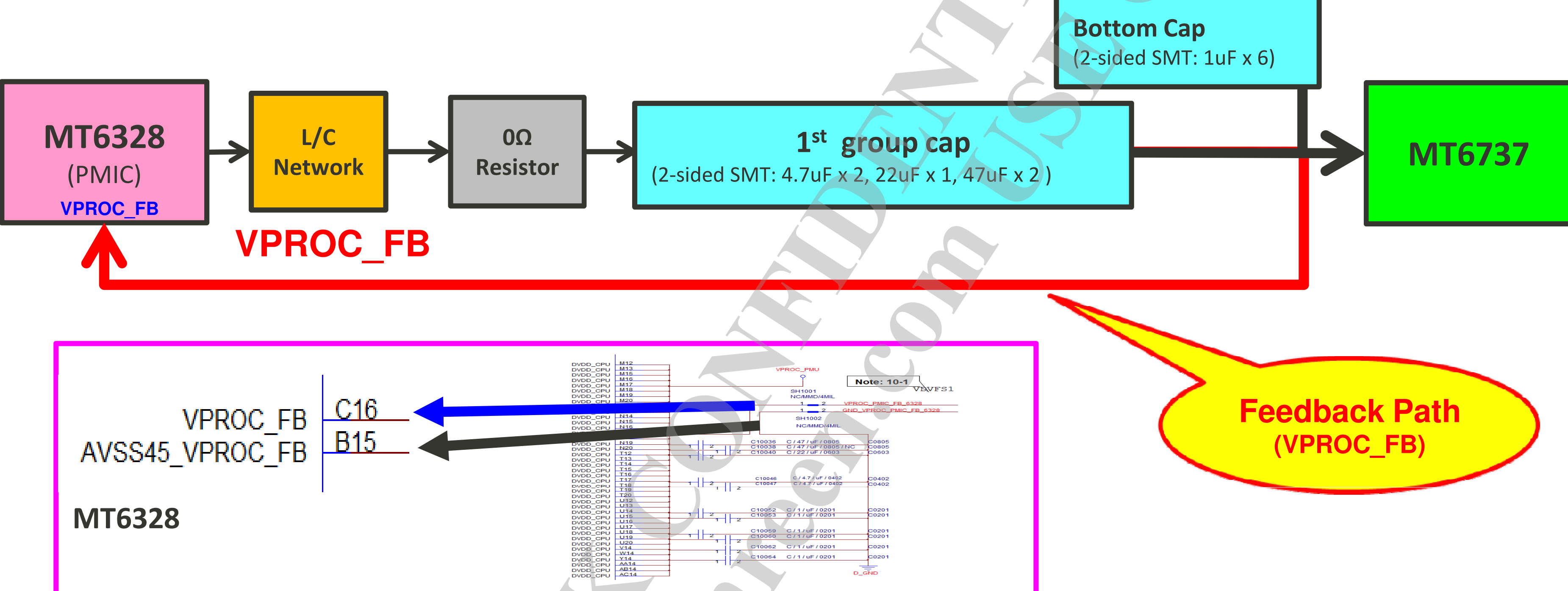
Guidelines for CPU Power: VPROC_FB



MT6737 provides a pair of feedback paths (VPROC_FB/GND_VPROC_FB) back to MT6328 (PMIC). Connect this pair feedback signals back to the backside caps.

These feedback signals are sensitive to coupled noise from other signals. Adopting ground shielding with enough GND vias is necessary.

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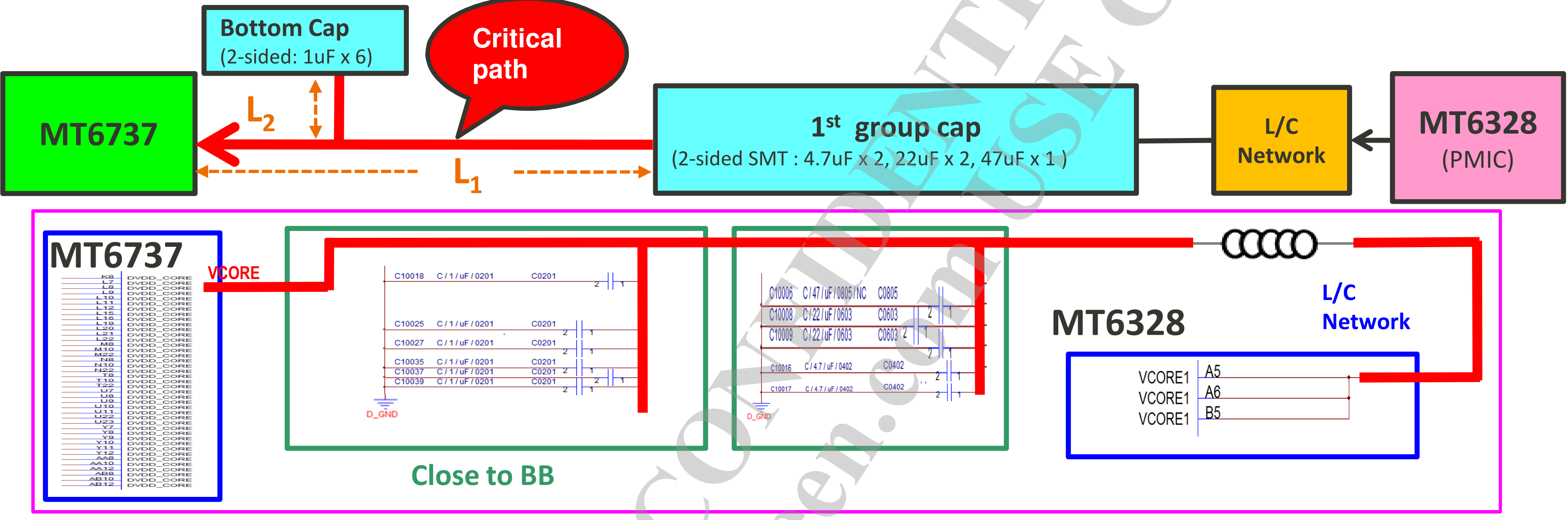
Guidelines for Core Power: VCORE



1. The whole PDN (power distribution network) is from MT6328 (PMIC) output pin, through first stage LC low pass filter, to the 1st group cap.
2. The "Critical-Path" is defined as the power trace segment from1st group cap to VCORE. The critical path design is strongly recommended to follow the given PCB layout guideline.
3. 2-sided SMT: Place six 1uF SMD capacitors as close to VCORE balls as possible. In "1st group cap" region, place two 4.7uF, two 22uF and one 47uF SMD capacitors.
   1) L_1 is defined as the critical path from "1st group cap" to MT6737 VCORE. The corresponding PCB routing rules are given as the following:
      - PWR adopts 1 layer PWR, L_1 length≤ 350mil; L_1 width≥ 100mil. Total 1 layer PWR & 1 layer GND (suggestion 1).
   2) L_2 is defined as the power trace segment from "Bottom cap" to MT6737. The corresponding PCB routing rules are given as the following:
      - Place six 1uF SMD capacitors right beneath the MT6737 VCORE and connect the SMD capacitors to wide power trace directly. Try to make L_2 as short as possible.

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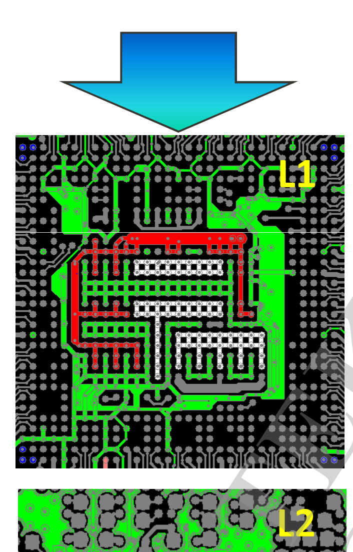
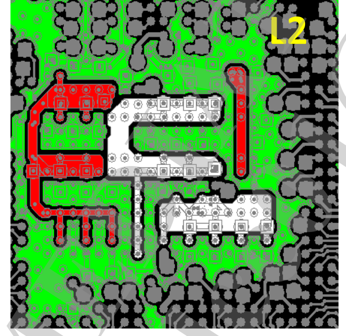
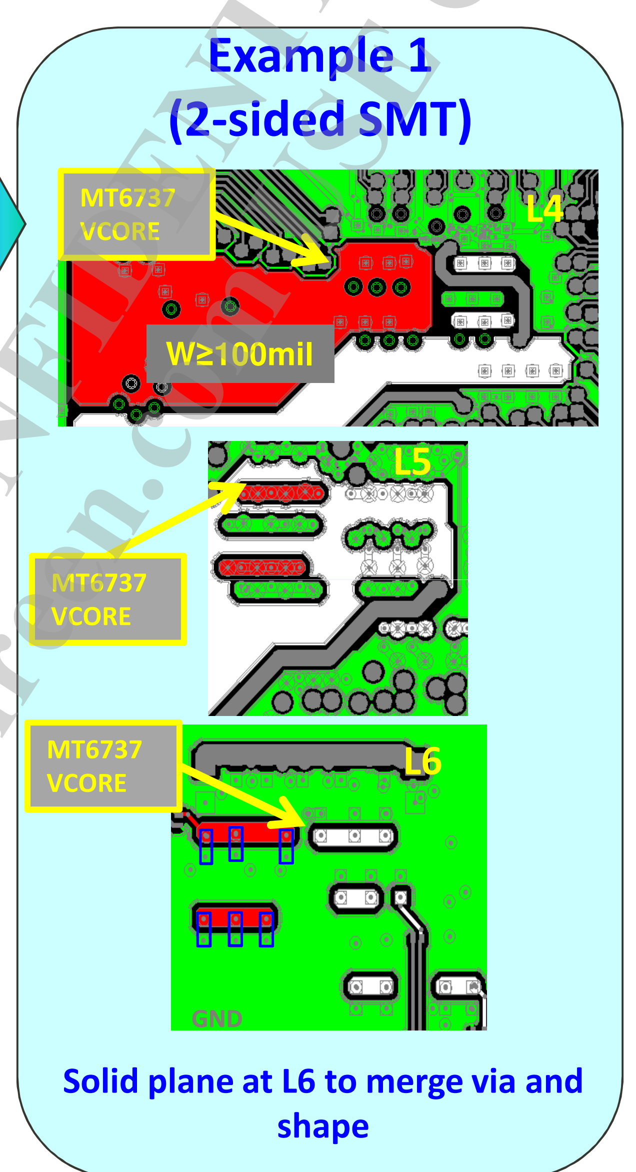
Guidelines for Core Power: VCORE

Design examples & suggestions” for the wide power trace from 1st group cap” to MT6737 VCORE：







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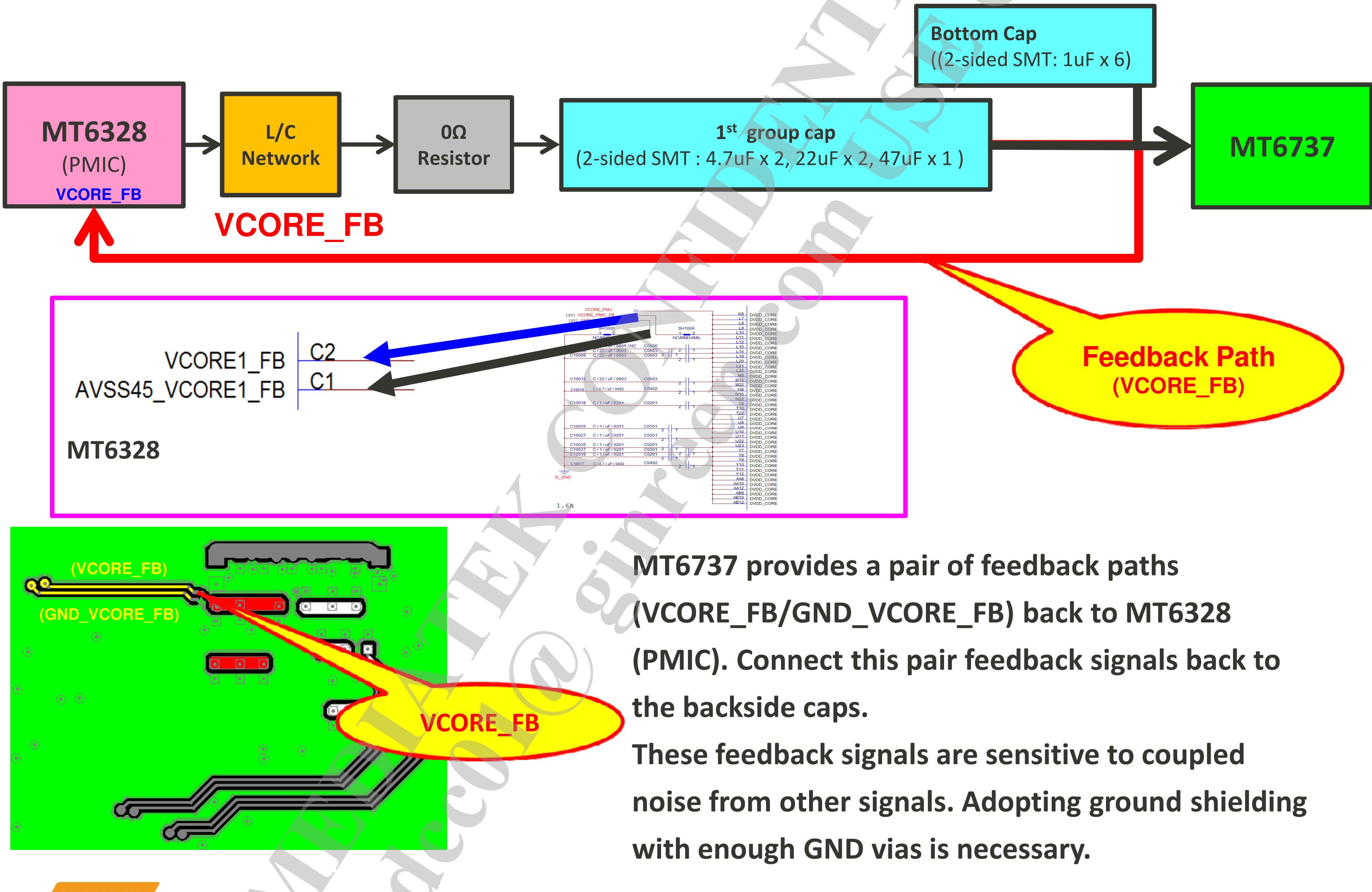
Guidelines for Core Power: VCORE_FB



MT6737 provides a pair of feedback paths (VCORE_FB/GND_VCORE_FB) back to MT6328 (PMIC). Connect this pair feedback signals back to the backside caps.

These feedback signals are sensitive to coupled noise from other signals. Adopting ground shielding with enough GND vias is necessary.

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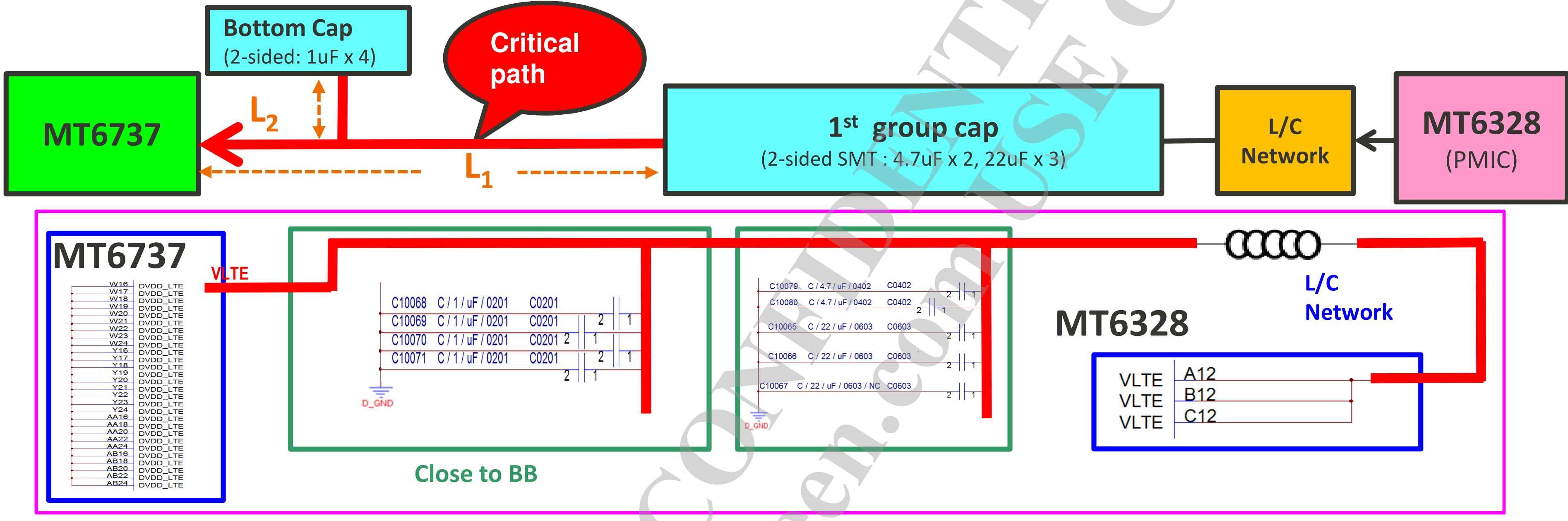
Guidelines for Core Power: VLTE



1. The whole PDN (power distribution network) is from MT6328 (PMIC) output pin, through first stage LC low pass filter, to the 1st group cap.
2. The "Critical-Path" is defined as the power trace segment from1st group cap to VLTE. The critical path design is strongly recommended to follow the given PCB layout guideline.
3. 2-sided SMT: Place four 1uF SMD capacitors as close as possible to VLTE balls. In "1st group cap" region, place two 4.7uF, two 22uF & one 47uF SMD capacitors.
   1) L_1 is defined as the critical path from "1st group cap" to MT6737 VCORE. The corresponding PCB routing rules are given as the following:
      - PWR adopts 1 layer PWR, L_1 length≤ 550mil; L_1 width≥ 80mil. Total 1 layer PWR & 1 layer GND (suggestion 1).
   2) L_2 is defined as the power trace segment from "Bottom cap" to MT6737. The corresponding PCB routing rules are given as the following:
      - Place four 1uF SMD capacitors right beneath the MT6737 VLTE, and connect the SMD capacitors to wide power trace directly. Try to make L_2 as short as possible.

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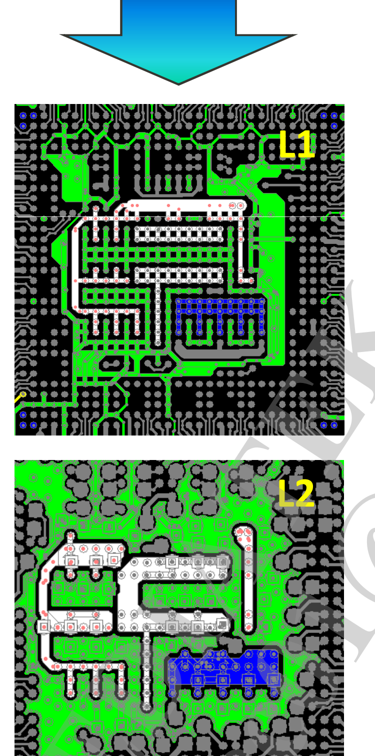
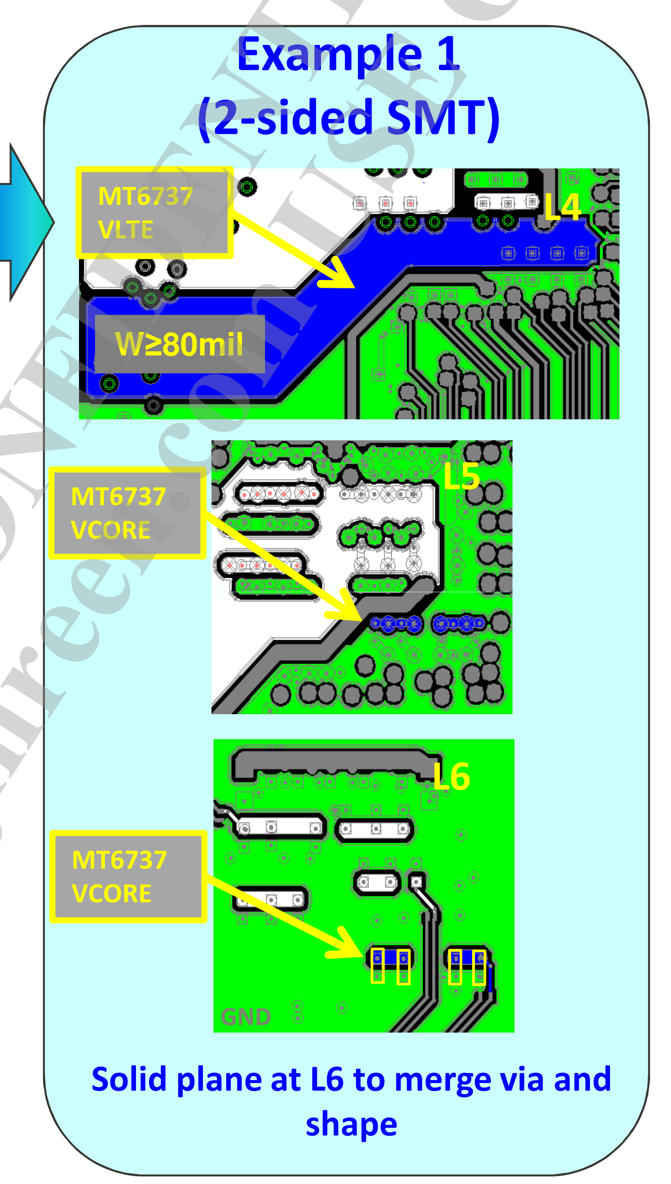
Guidelines for Core Power: VLTE

Design examples & suggestions" for the wide power trace from 1st group cap" to MT6737 VLTE：





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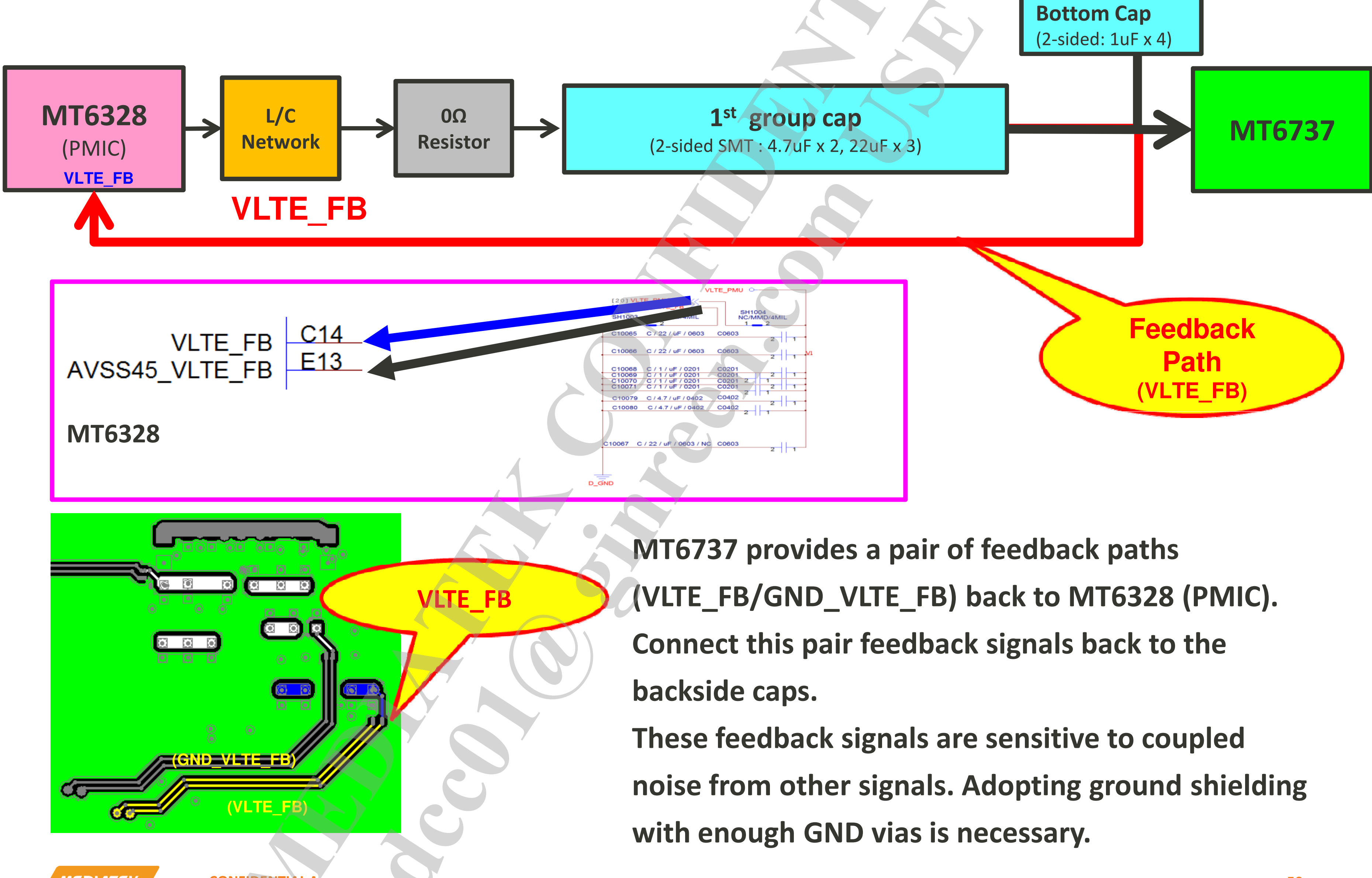
Guidelines for Core Power: VLTE_FB



MT6737 provides a pair of feedback paths (VLTE_FB/GND_VLTE_FB) back to MT6328 (PMIC). Connect this pair feedback signals back to the backside caps.

These feedback signals are sensitive to coupled noise from other signals. Adopting ground shielding with enough GND vias is necessary.

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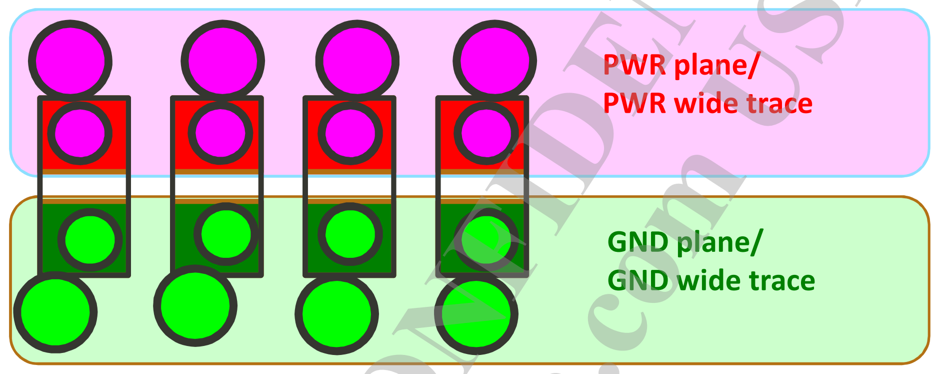
Via Interconnection



- **Design suggestions for via interconnection**

  1. Via interconnect is critical in delivering current between each layer and is usually the bottleneck in the entire PDN networking. Thus, we strongly recommend you follow the related PWR/GND layout guidelines.
  2. PWR/GND via is recommended to connect to the "wide power trace" and placed as close to the decoupling capacitor as possible.
  3. Each decoupling capacitor should have at last one pair PWR/GND via. If the routing space is available, more PWR/GND vias are recommended. The ratio of Pad: Laser via: PTH via =1: 1: 1. Try to distribute PTH & Laser vias uniformly.

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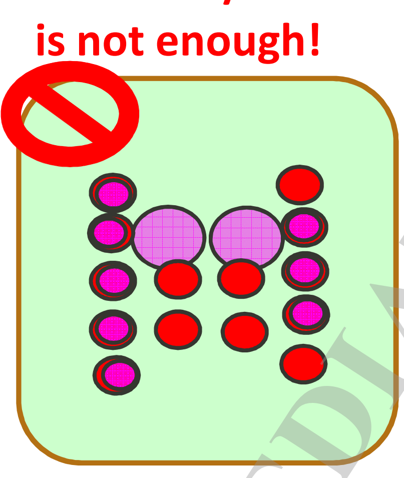
Via Interconnection

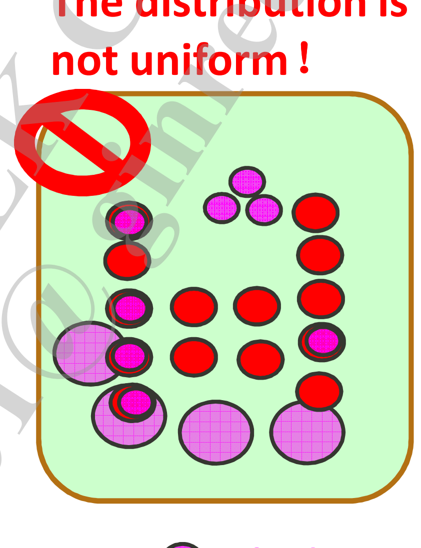
- **Design suggestions of VPROC/VCORE/VLTE via interconnection in PCB:** (Top view of MT6737 PCB)

1. **The # of blind via & PTH via beneath the VPROC region should meet the requirement. Taking MT6737 for example, the minimum requirement is 6 blind vias & 6 PTH vias.**
2. **The # of blind via & PTH via beneath the VCORE region should meet the requirement. Taking MT6737 for example, the minimum requirement is 6 blind vias & 6 PTH vias.**
3. **The # of blind via & PTH via beneath the VLTE region should meet the requirement. Taking MT6737 for example, the minimum requirement is 4 blind vias & 4 PTH vias.**
4. **More blind vias are recommended. Use the "via on ball" process " on VPROC/VCORE ball" and directly connect it to the wide power trace & PTH via. In addition, make sure the blind vias & PTH vias are uniformly distributed.**
5. **It is better to place GND vias as close to PWD vias as possible as shown in figure below. Basically, adding the # of GND via is helpful in reducing PWR/GND inductance.**

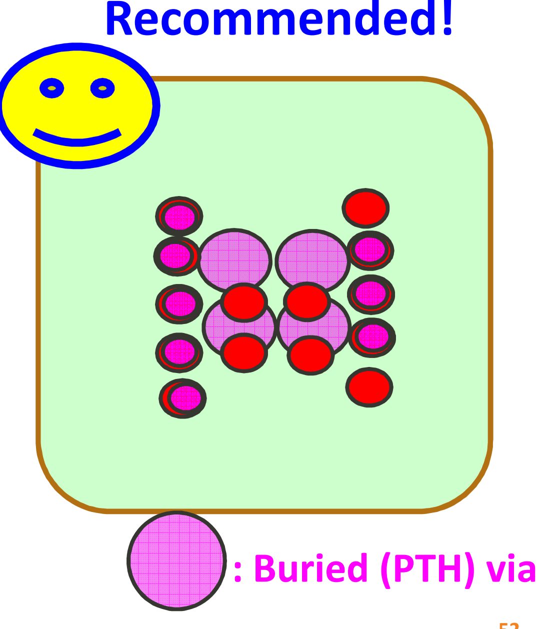
# of blind/PTH via is not enough!



The distribution is not uniform !



Recommended!



:VPROC/VCORE/VLTE (PWR balls)

:Blind Via

: Buried (PTH) via

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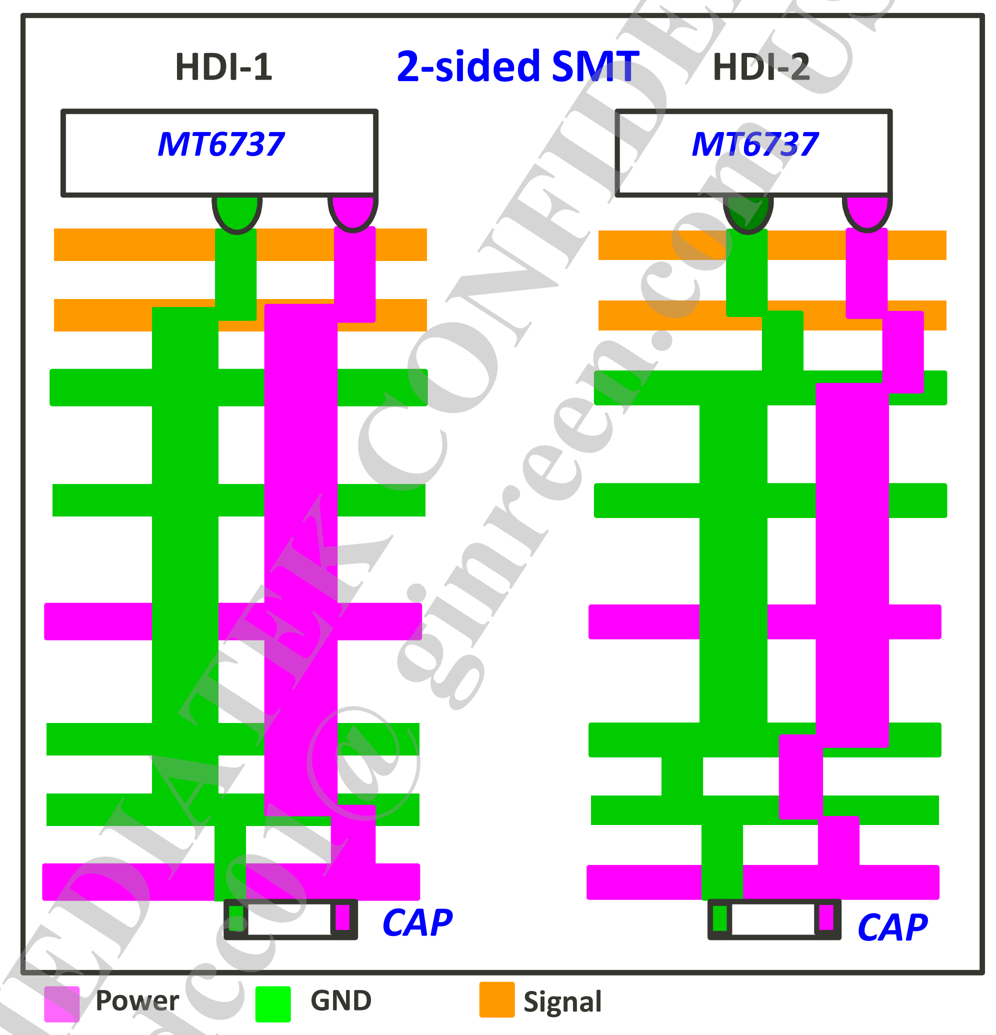
Via Interconnection

1. Place GND vias as close to PWD vias as possible to reduce PWR/GND inductance.
2. The ratio of "# of GND via: # of PWR via" is recommended to be 1:1.



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Outlines

- **Brief Introduction to MT6737**
- **Packaging**
  - Package Outline of MT6737
  - MT6737 Footprint Recommendation
  - MT6737 Ball Out Design
- **General Guidelines**
  - PCB Stack-up Recommendation
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  - Placement Notes
  - MT6737 Fan Out
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  - LPDDR3
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- **Others**
  - MT6737 RF Interface - MT6169 - MT6158
  - MT6328 (PMU)
  - MT6625 (BT/FM/WiFi/GPS)
  - USB/MIPI/SIM Card/T-Card/eMMC/Differential Pair Layout Suggestion

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MT6169
PCB Layout Guideline

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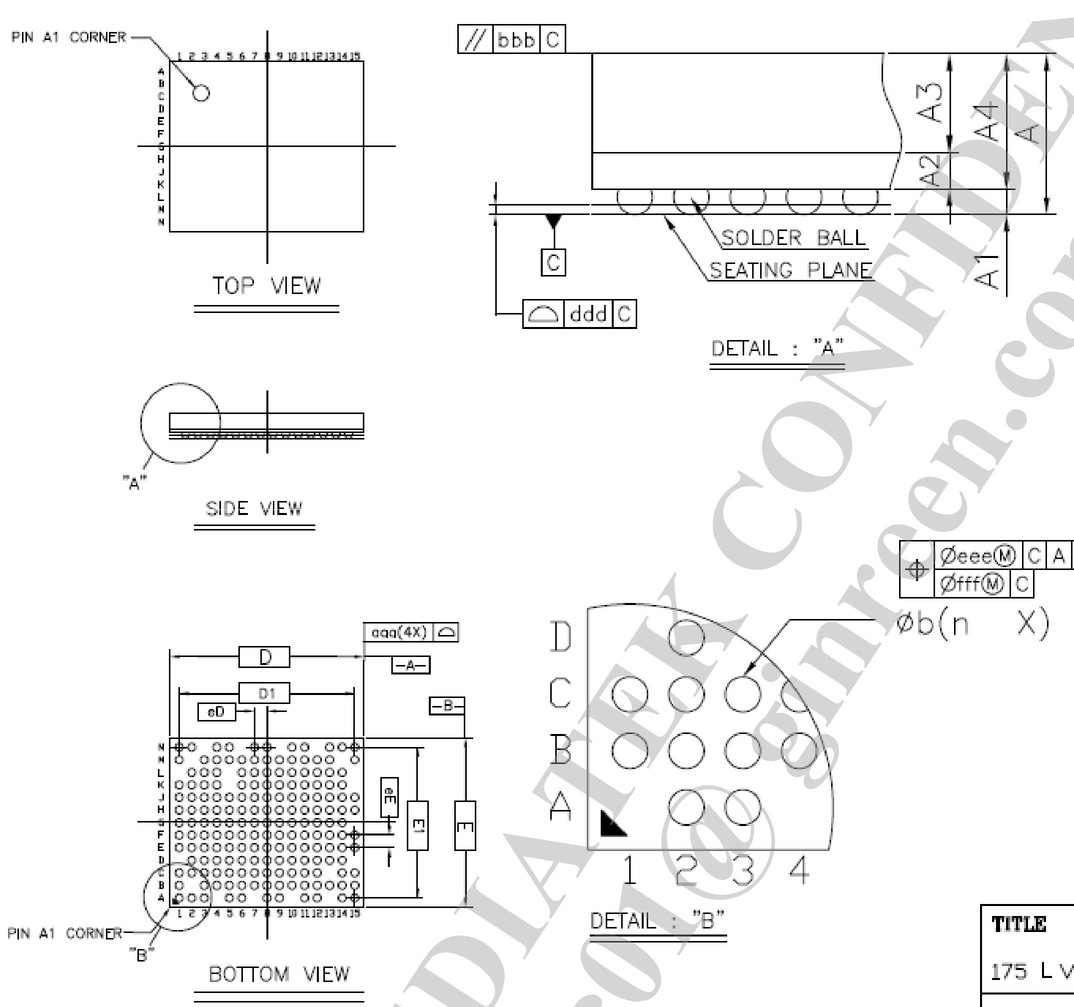
Package Outline of MT6169



Item		Symbol	Common Dimensions MIN.	NOM.	MAX.
Package Type				VSSP	
Body Size	X	D	6.10	6.20	6.30
	Y	E	5.30	5.40	5.50
Ball Pitch	X	eD		0.40	
	Y	eE		0.40	
Total Thickness		A	–	–	0.90
Mold Thickness		A3		0.53 Ref.	
Substrate Thickness		A2		0.11 Ref.	
Substrate+Mold Thickness		A4	0.59	0.64	0.69
Ball Diameter				0.25	
Stand Off		A1	0.12	0.16	0.20
Ball Width		b	0.20	0.25	0.30
Package Edge Tolerance		aaa	0.05		
Mold Flatness		ccc	0.10		
Coplanarity		ddd	0.08		
Ball Offset (Package)		eee	0.15		
Ball Offset (Ball)		fff	0.05		
Ball Count		n	175		
Edge Ball Center to Center	X	D1	5.60		
	Y	E1	4.80		

TITLE PACKAGE OUTLINE 175 L VSSP 6.2X5.4X0.90		MEDIATEK	
DWG. NO.	REV.	SHEET	UNIT
---	A	2 OF 2	MM

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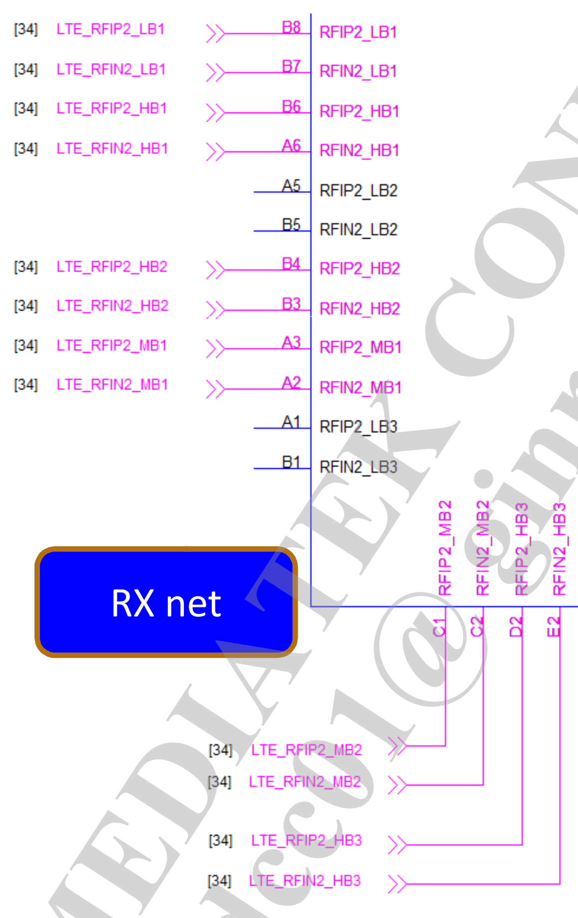
MT6169 Ball Map

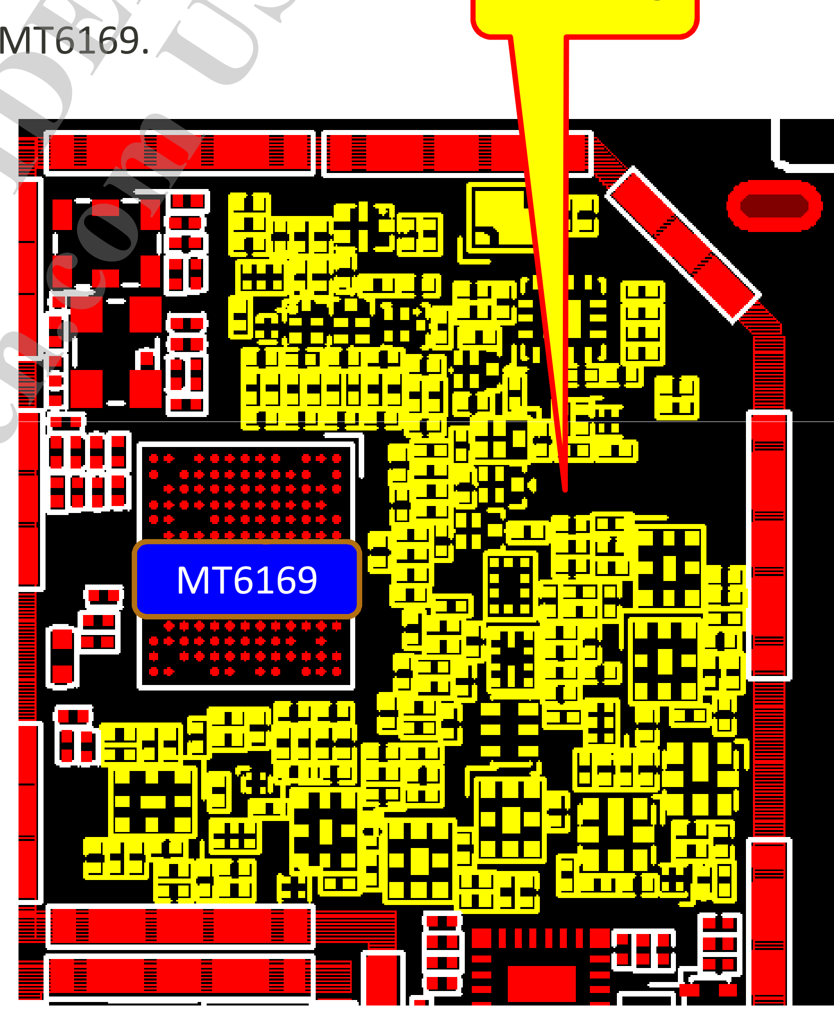
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
A	RFIP2_LB3	RFIN2_MB1	RFIP2_MB1		RFIP2_LB2	RFIN2_HB1		RFIN1_HB3	RFIP1_HB3		RFIP1_LB3	RFIN1_HB2		RFIN1_LB2	RFIP1_LB2
B	RFIN2_LB3		RFIN2_HB2	RFIP2_HB2	RFIN2_LB2	RFIP2_HB1	RFIN2_LB1	RFIP2_LB1	RFIN1_MB2	RFIP1_MB2	RFIN1_LB3	RFIP1_HB2	RFIN1_MB1	RFIP1_MB1	RFIN1_HB1
C	RFIP2_MB2	RFIN2_MB2	GND	GND	GND	GND	GND	VRXHF2	GND	GND	GND	GND		RFIN1_LB1	RFIP1_HB1
D		RFIP2_HB3	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	VRXHF1	RFIP1_LB1	
E	GND	RFIN2_HB3	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	TXO_GND	TXO_GND	TXO_GND
F	OUT_32K	GND	TST1	GND	GND	GND	GND	GND	GND	GND	GND	GND	TXO_GND	TX_HB2	TX_HB1
G	XO3	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	TXO_GND	TX_MB1	
H	XO2	XO4	GND	GND	GND	GND	GND	GND	GND	GND	GND	TST4	TXO_GND	TX_MB2	TX_[illegible]
J	VTCXO	32K_EN	GND	GND	BSI_D1	BSI_D0	BSI_EN	GND	GND	GND	GND	GND	TXO_GND	TX_LB2	TX_LB3
K	XTAL2	XTAL1	GND	BSI_D2		BSI_CK	GND	GND	GND	TXBPI	VTXLF	GND	TXO_GND	TX_LB1	
L		XMODE	GND	VDC[illegible]_DIG		GND	GND	GND	GND	GND	GND	GND	DET_GND	TXO_GND	
M	XO1		VIO	[illegible]_BBQP	RX2_BBIP	RX1_BBQP	RX1_BBQN	VRXLF	TMEAS	TST2	V28_ESD1	TST3	TXDET		TX_BBIP
N	CLK_SEL	EN_26M_BB		RX2_BBQN	RX2_BBIN		RX1_BBIN	RX1_BBIP		VRT	VTXHF		TX_BBQP	TX_BBQN	TX_BBIN

CONFIDENTIAL A

MT6169 Placement (1/2)

- For 5M12B, RF RX needs two receiver circuits, DRX (Diversity RX) and PRX (Primary RX).
- RX net matching component should be placed near MT6169.





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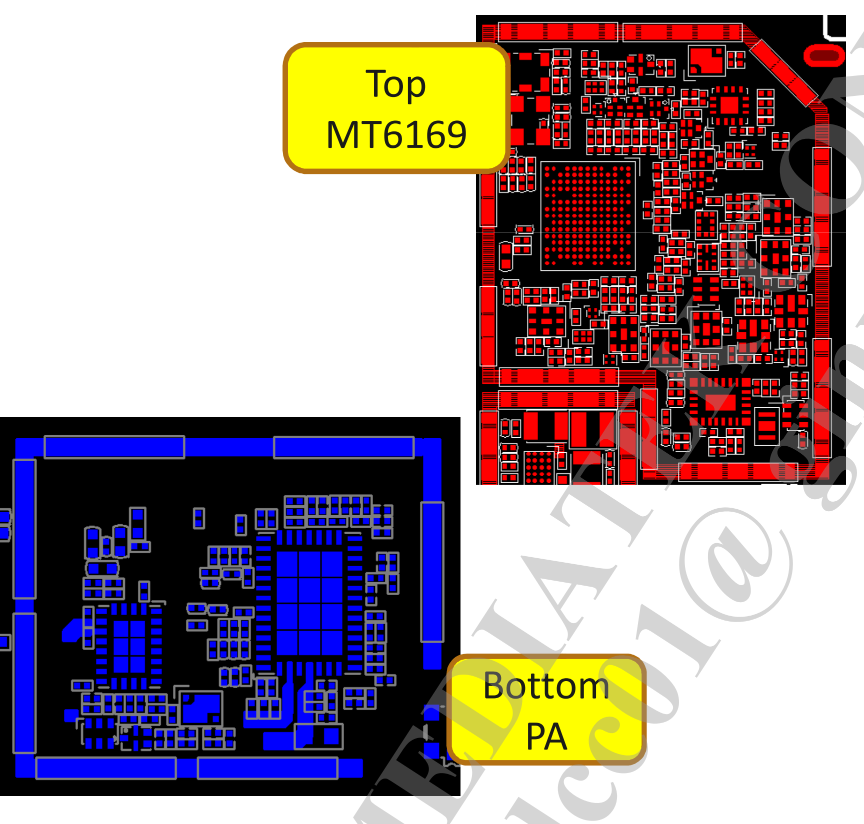
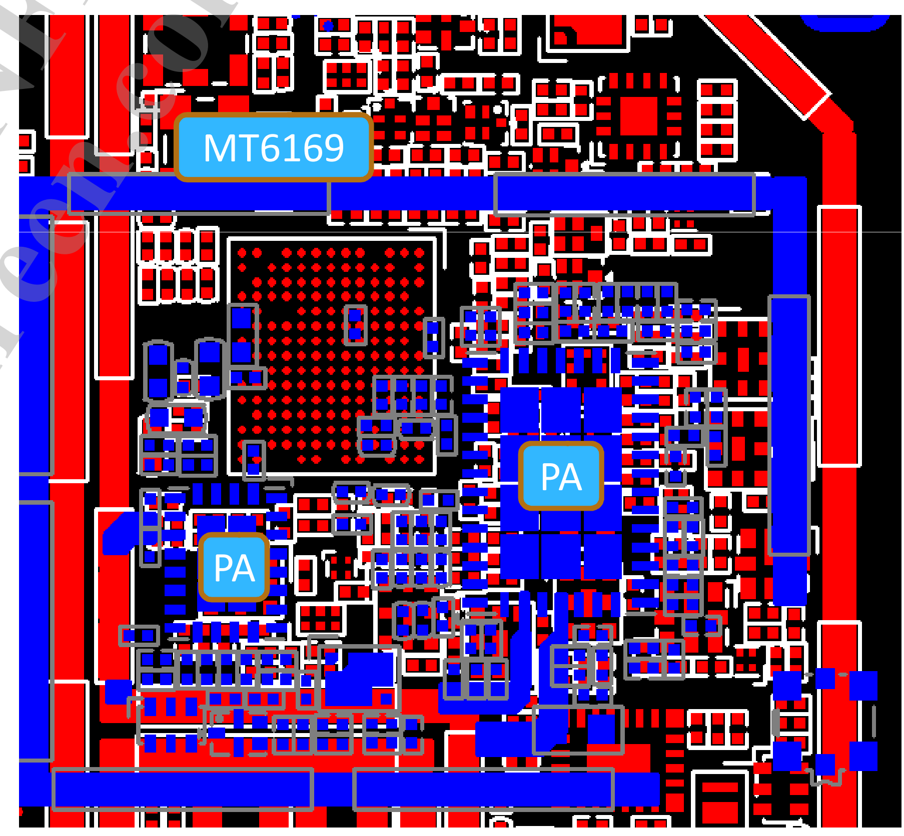
MT6169 Placement (2/2)

- MT6169 and PA IC should have their own shielding case to prevent de-sense issues. MT6169 and PA should not be overlapped when placed in different layers.
- Have GND plane at L1 in RF shielding case and give more GND vias to connect to the main GND plane. Also give more GND vias on PA Epad to avoid the thermal issue.





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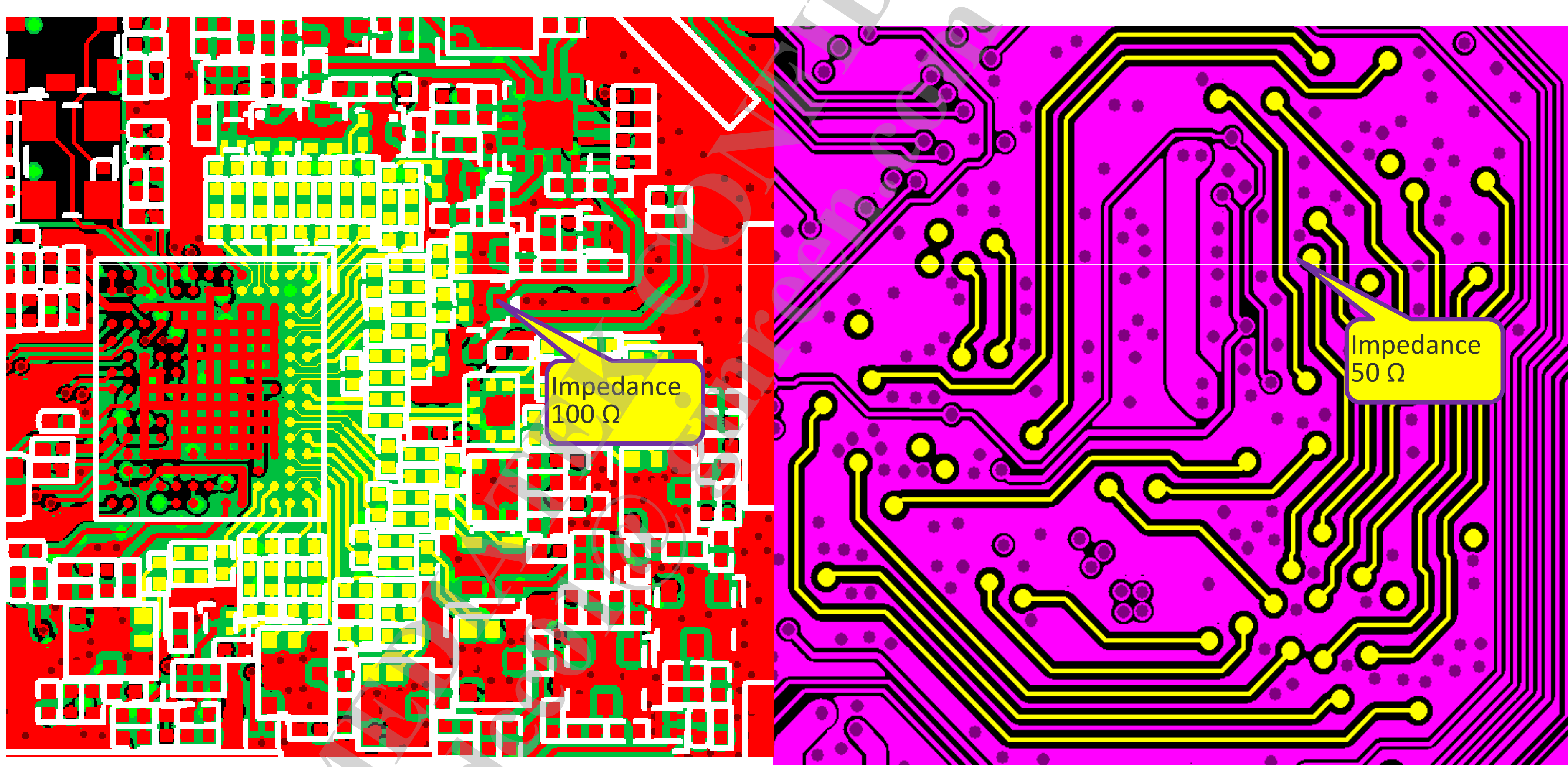
MT6169 TX/RX Signals

- Impedance control is necessary for all RF signals.
- Make sure that the routing impedance is single-ended 50Ω for TX/PDET/RX and differential 100Ω for RX traces.



MEDIATEK CONFIDENTIAL A

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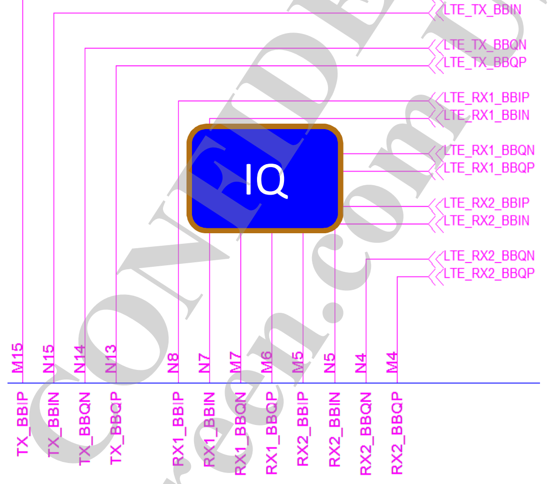
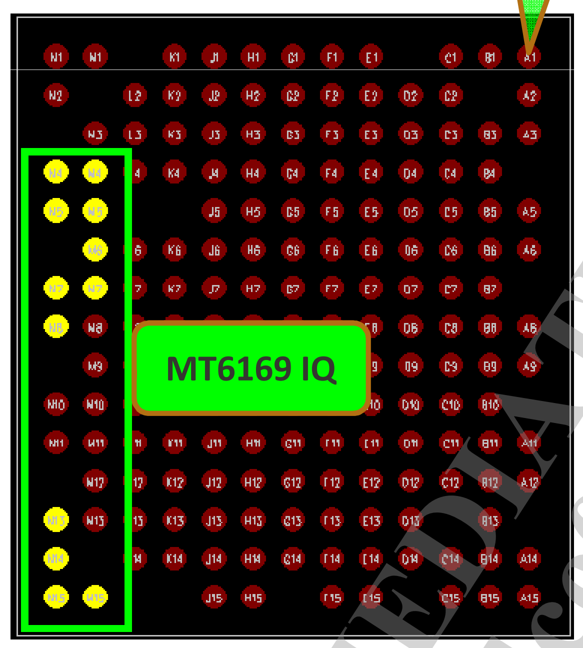
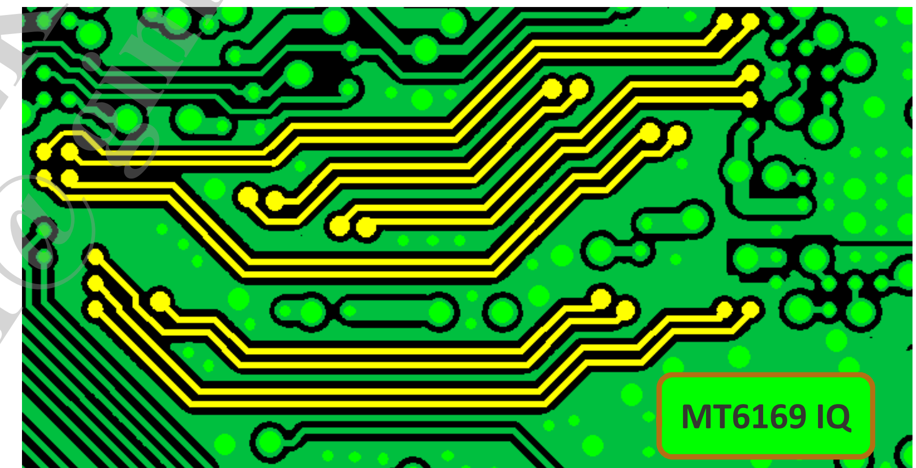
MT6169 IQ Signals

- I/Q signals are differential pairs and should be shielded by GND (adjacent up/down layers).

PCB Net Name	IC Ball Number
LTE_TX_BBIP	AK2
LTE_TX_BBIN	AK3
LTE_TX_BBQP	AL3
LTE_TX_BBQN	AK4
LTE_RX1_BBIP	AH7
LTE_RX1_BBIN	AJ7
LTE_RX1_BBQP	AK6
LTE_RX1_BBQN	AL6
LTE_RX2_BBIP	AK7
LTE_RX2_BBIN	AK8
LTE_RX2_BBQP	AJ8
LTE_RX2_BBQN	AH8







MT6169 Duplexer

- **Duplexer notice:**

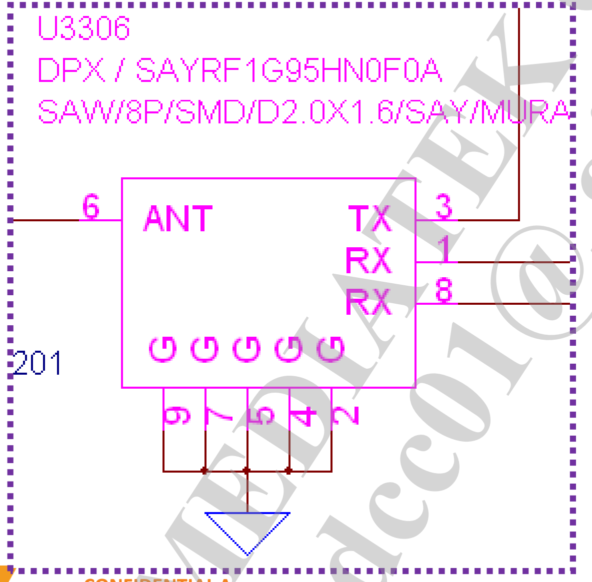
a. Enlarge L1 copper pouring range for duplexer GND pins (2, 4, 5, 7, 9).

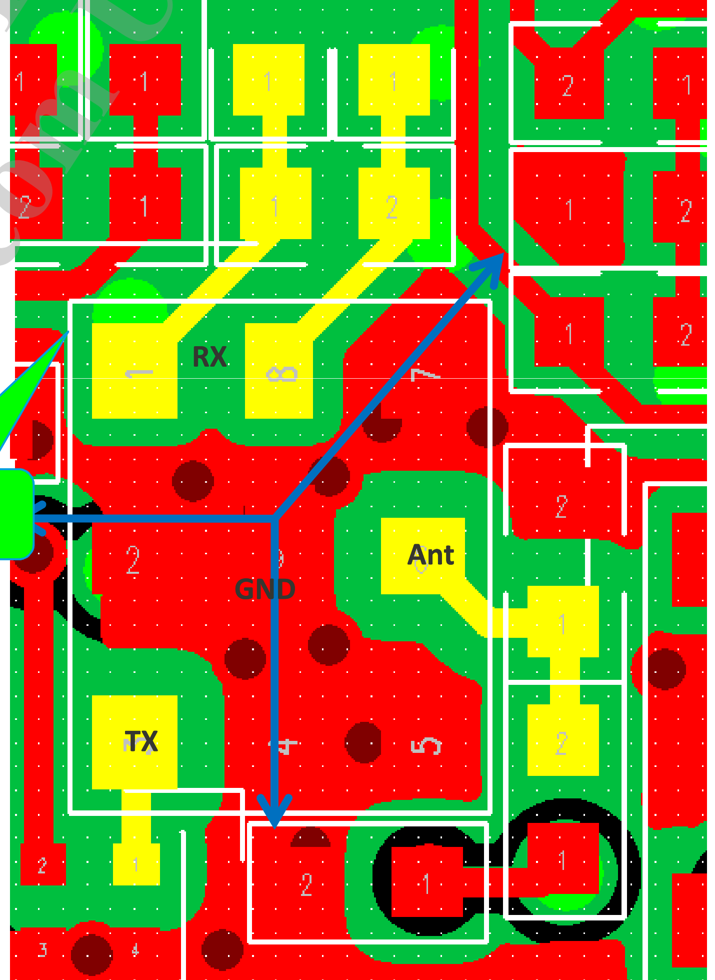
b. Avoid parallel routing between ANT/RX/TX signals.

c. Maintain good isolation between ANT/RX/TX by:
   1. GND shielding between these three path.
   2. Good grounding with plenty of GND via.

d. There should be good GND plane at L2 for reference.

e. If there are TX signals in the inner layer, isolate TX pin from others signals by GND.





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MT6169 Crystal

- 26MHz crystal should have good GND shielding at L1 (Fig.1).
- Keep out the region below 26MHz crystal pin4 at L2.
- There should be good GND plane at L3 for reference (Fig.2).

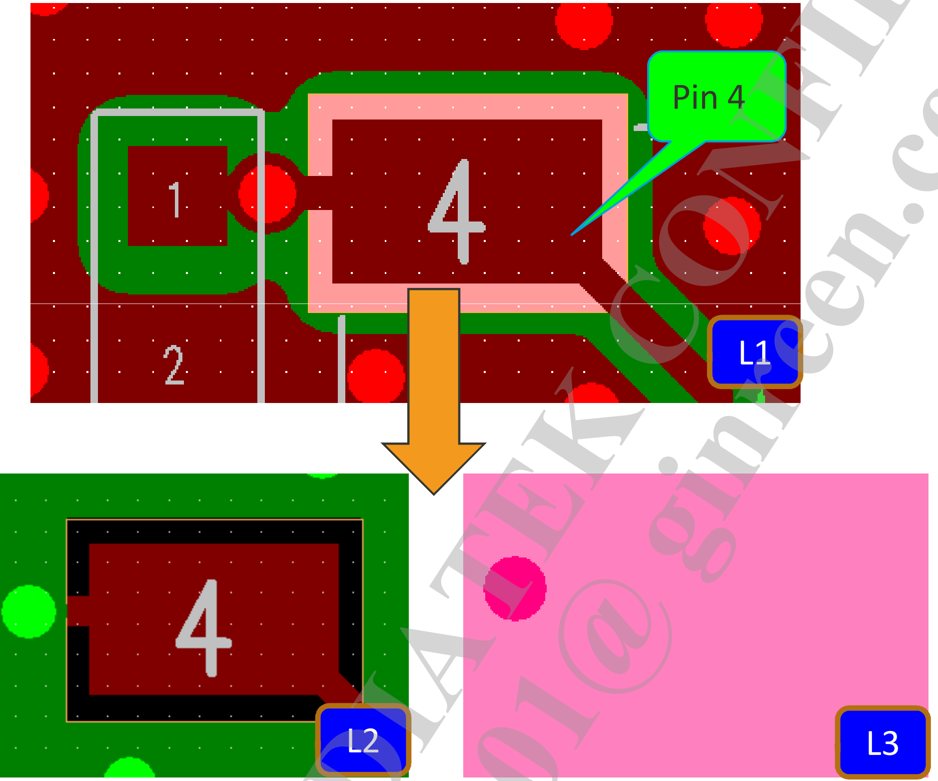

Fig.2

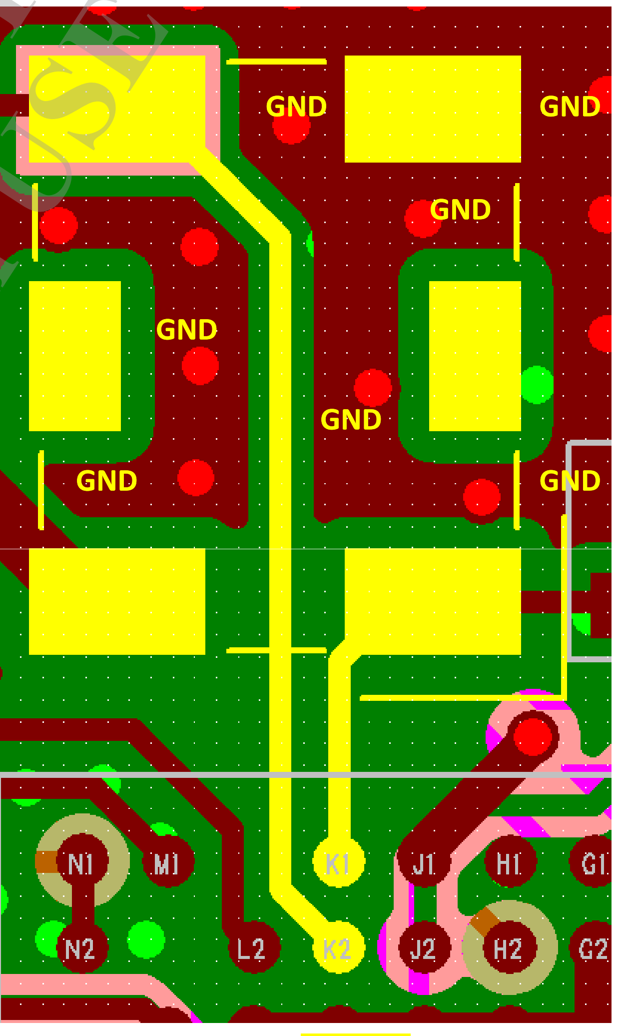

Fig.1

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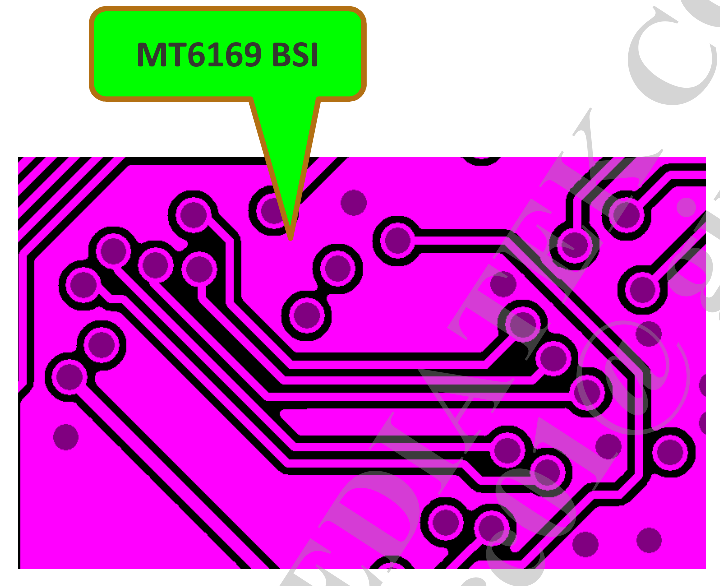
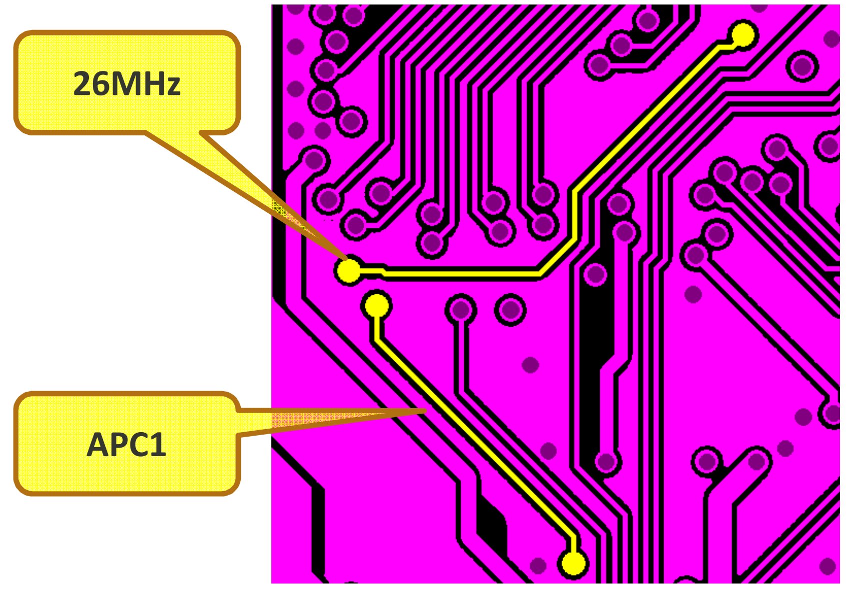
MT6169 Others

- BSI signals should have GND shielding by group (adjacent up/down layers).
- LTE 26MHz (AE10) & APC1 (AH10 ball) should have GND shielding by group (adjacent up/down layers).
- AUXADC_REF_RF&THERM_SENSE should be routed as diff. pairs and with 24mil AUXADC_GND signals in the under layer.

PCB Net Name	IC Ball Number
LTE_RFIC0_BSI_EN	M33
LTE_RFIC0_BSI_CK	L32
LTE_RFIC0_BSI_D2	M32
LTE_RFIC0_BSI_D1	L33
LTE_RFIC0_BSI_D0	L31





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Outlines

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  - MT6328 (PMU)
  - MT6625 (BT/FM/WiFi/GPS)
  - USB/MIPI/SIM Card/T-Card/eMMC/Differential Pair Layout Suggestion

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MT6158
PCB Layout Guideline

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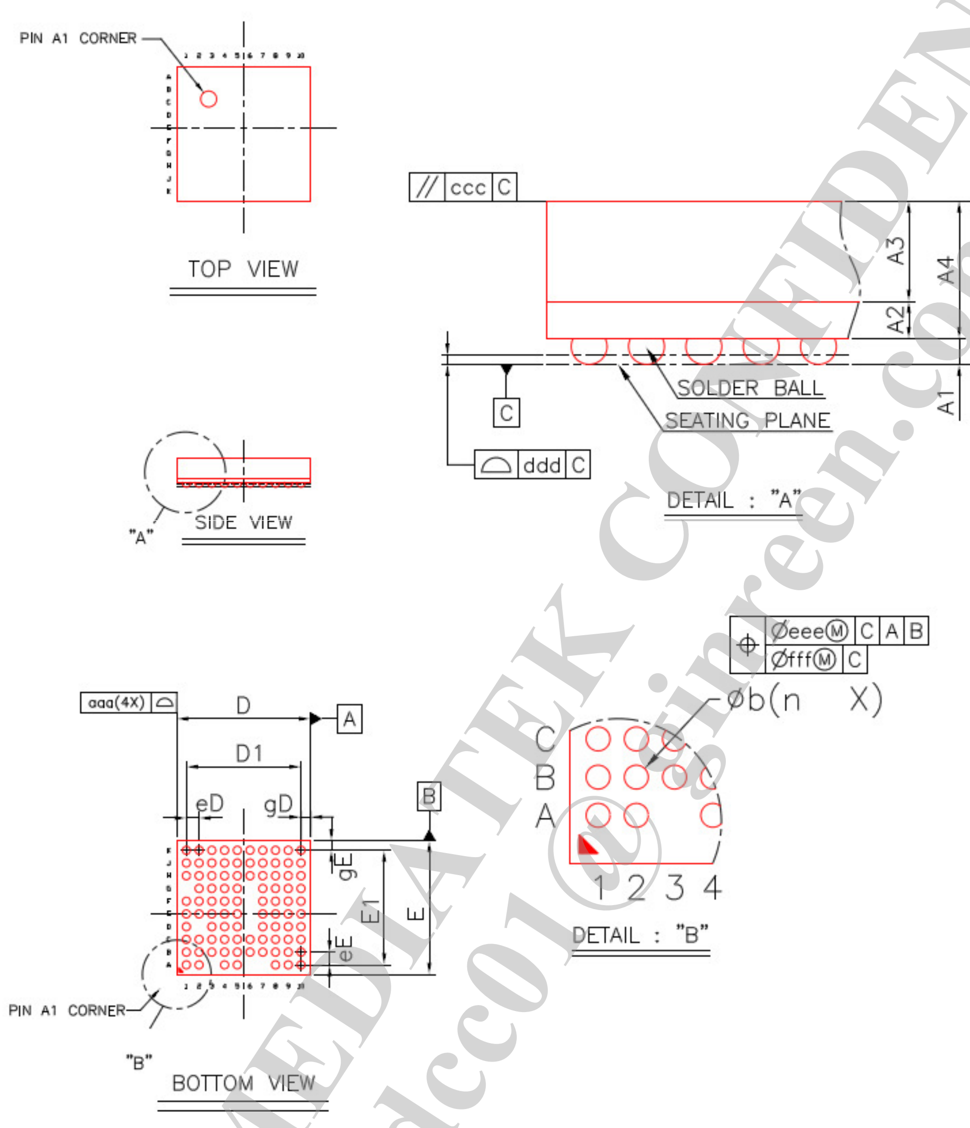
Package Outline of MT6158



Item		Symbol	Common Dimensions MIN.	NOM.	MAX.
Package Type				VFBGA	
Body Size	X	D	4.10	4.20	4.30
	Y	E	4.10	4.20	4.30
Ball Pitch	X	eD		0.40	
	Y	eE		0.40	
Mold Thickness		A3		0.65 Ref.	
Substrate Thickness		A2		0.11 Ref.	
Substrate+Mold Thickness		A4	0.71	0.76	0.81
Total Thickness		A	–	–	1.00
Ball Diameter				0.25	
Ball Stand Off		A1	0.12	0.16	0.20
Ball Width		b	0.20	0.25	0.30
Package Edge Tolerance		aaa		0.05	
Mold Flatness		ccc		0.10	
Coplanarity		ddd		0.08	
Ball Offset (Package)		eee		0.15	
Ball Offset (Ball)		fff		0.05	
Ball Count		n		91	
Edge Ball Center to Center	X	D1		3.60	
	Y	E1		3.60	
Edge Ball Center to Package Edge	X	gD		0.30	
	Y	gE		0.30	

TITLE	PACKAGE OUTLINE VFBGA 91 L 4.2X 4.2X 1.00mm		MEDIATEK
DWG. NO.	REV.	SHEET	UNIT

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MT6158 Ball Map

RF RX

RF TX

	1	2	3	4	5	6	7	8	9	10	
A	VRXHF	RXVCO1_MON	DP	LNA_HB1_RXP	LNA_HB2_RXP	DP	DP	LB_TX	HB1_TX	HB2_TX	A
B	LNA_HB2_DRXN	LNA_LB_RXP	LNA_LB_RXN	LNA_HB1_RXN	LNA_HB2_RXN	GND	GND	GND	GND	VTXHF	B
C	LNA_HB2_DRXP	GND	GND	GND	GND	GND	GND	GND	DETGND	TMEAS	C
D	LNA_HB1_DRXP	DP	GND	GND	BSI_CLK	DP	GND	GND	V28	DET	D
E	LNA_HB1_DRXN	RXVCO2_MON	GND	GND	BSI_DATA	DP	TX_BSI_CLK	GND	GND	TX_QN	E
F	LNA_LB_DRXN	LNA_LB_DRXP	GND	GND	BSI_EN	DP	TX_BSI_DATA	GND	TX_IP	TX_QP	F
G	DP	DCXO_32KEN	GND	GND	GND	DP	TX_BSI_EN	GND	TX_IN	TST1	G
H	EN_BB	GND	GND	GND	GND	GND	GND	GND	TST2	VTXLF	H
J	XTAL2	OUT_32K	XMODE	RCAL	VXODIG	DRX_IN	DRX_QP	RX_IP	RX_IN	TX_BPI	J
K	XTAL1	VTCXO28	REFCLK	VIO18	VRXLF	DRX_IP	DRX_QN	RX_QN	RX_QP	TXVCO_MON	K
		2	3	4	5	6	7	8	9	10	

C2K TX IQ

26MHz Crystal

32K Clock

C2K BSI

C2K RXIQ

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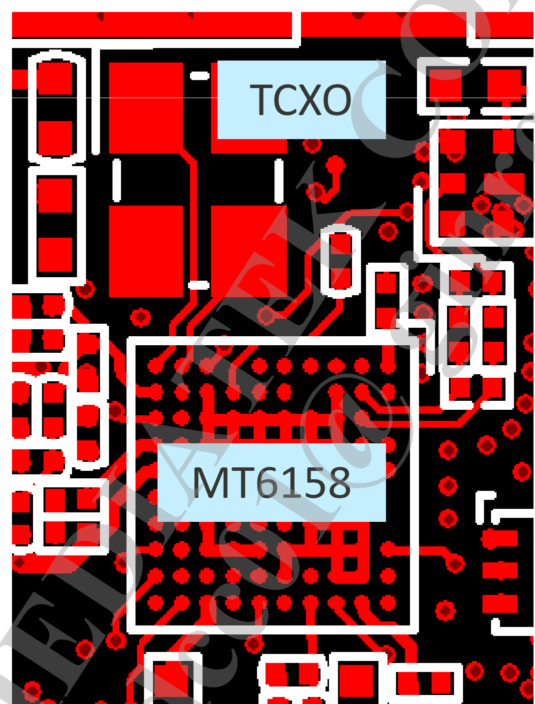
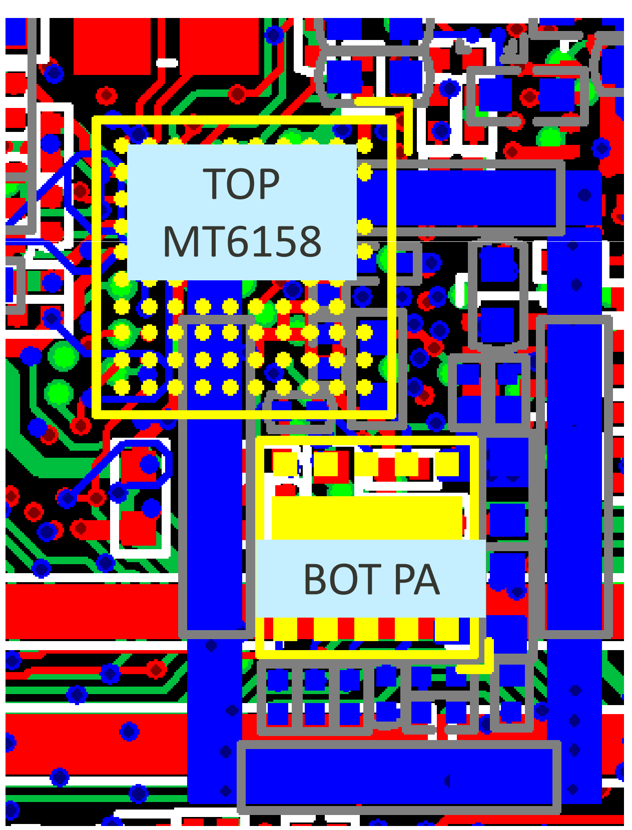
MT6158 Placement

- MT6158 and PA IC should have their own shielding case to prevent de-sense issues. MT6158 and PA should not be overlapped when placed in different layers.
- Have GND plane at L1 in RF shielding case and give more GND vias to connect to the main GND plane. Also give more GND vias on PA Epad to avoid thermal issues.
- RX components should have good isolation with antenna.
- TCXO should be placed near MT6158 and dig out L2 GND plane under TCXO.





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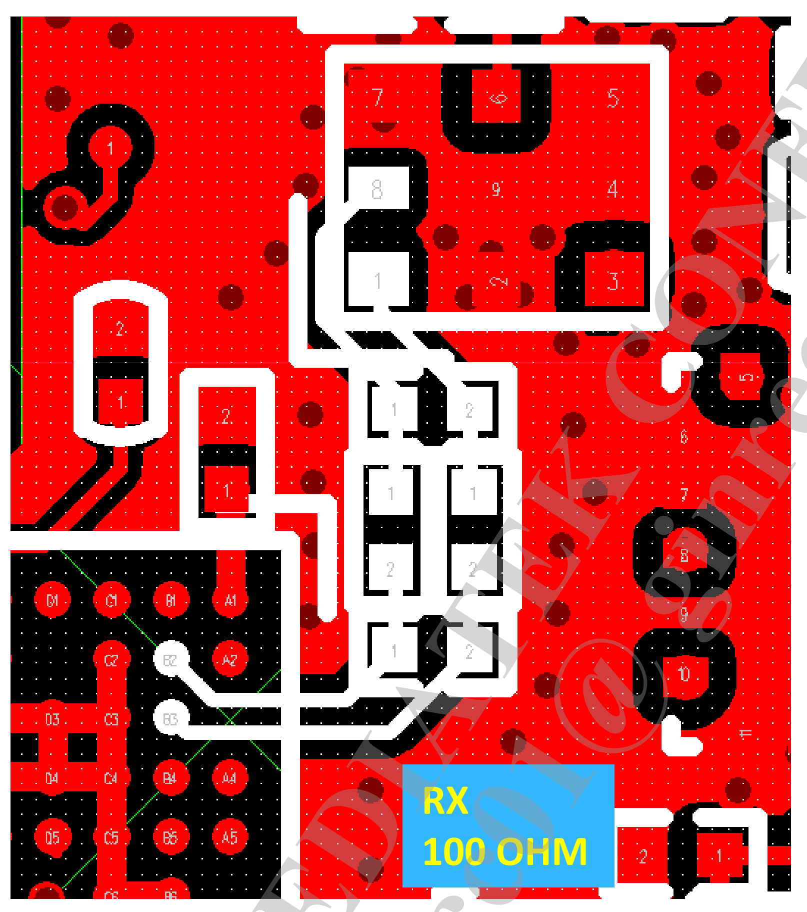
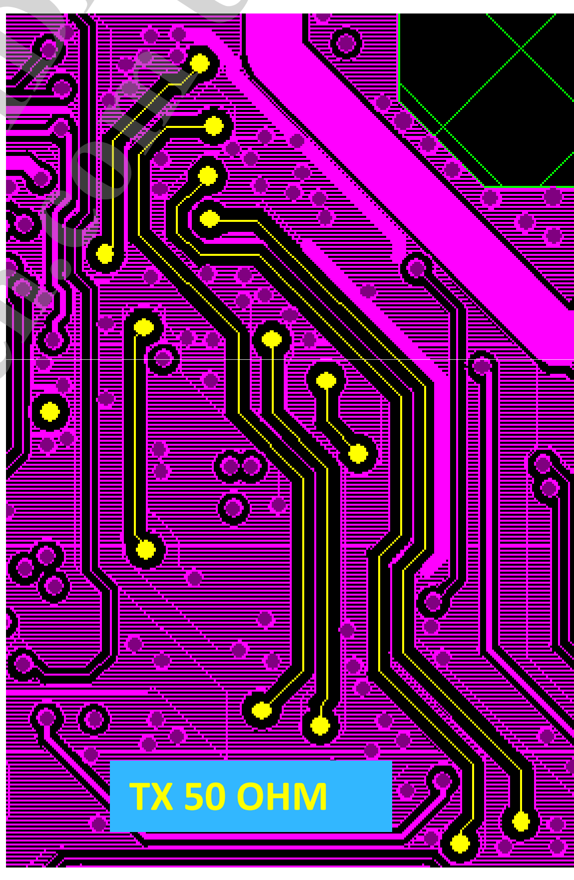
MT6158 TX/RX Signals

- Impedance control is necessary for all RF signals, single-ended 50Ω for TX signals and differential 100Ω for RX signals.





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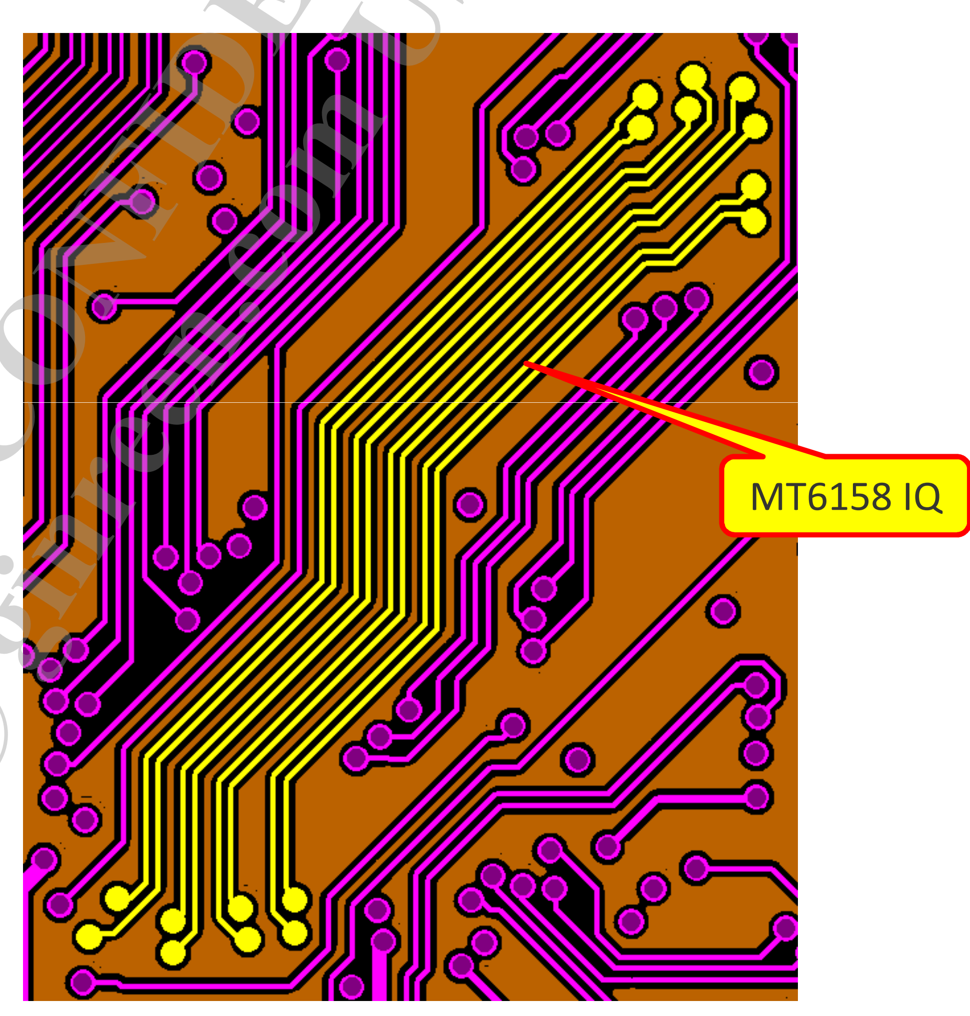
MT6158 IQ Signals

- I/Q signals are differential pairs and should be shielded by GND (adjacent up/down layers).

PCB Net Name	IC Ball Number
TX_BBIP_C2K	F9
TX_BBIN_C2K	G9
TX_BBQP_C2K	F10
TX_BBQN_C2K	E10
RX_BBIP_C2K	J8
RX_BBIN_C2K	J9
RX_BBQP_C2K	K9
RX_BBQN_C2K	K8
DRX_BBIP_C2K	K6
DRX_BBIN_C2K	J6
DRX_BBQP_C2K	J7
DRX_BBQN_C2K	K7



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MT6158 Others

- Two group BSI signals in Fig.1 should be shielded by GND by groups (adjacent up/down layers).
- C2K_26M_IN should be shielded by GND (adjacent up/down layers).
- Duplexer layout notice is the same as MT6169.

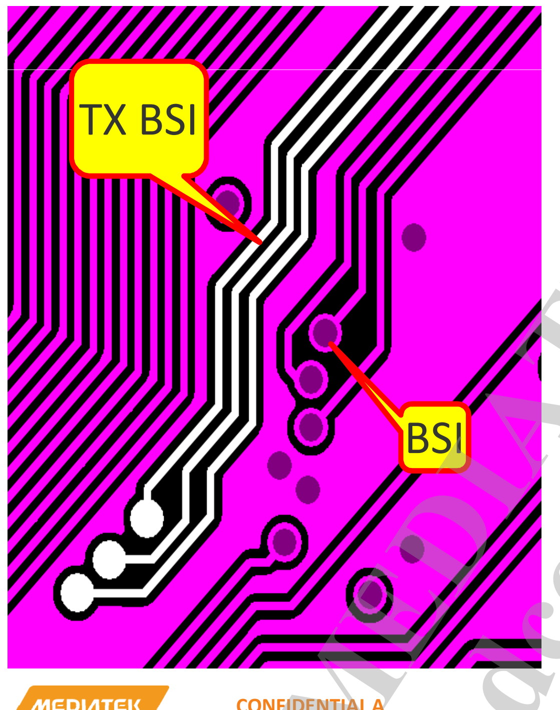
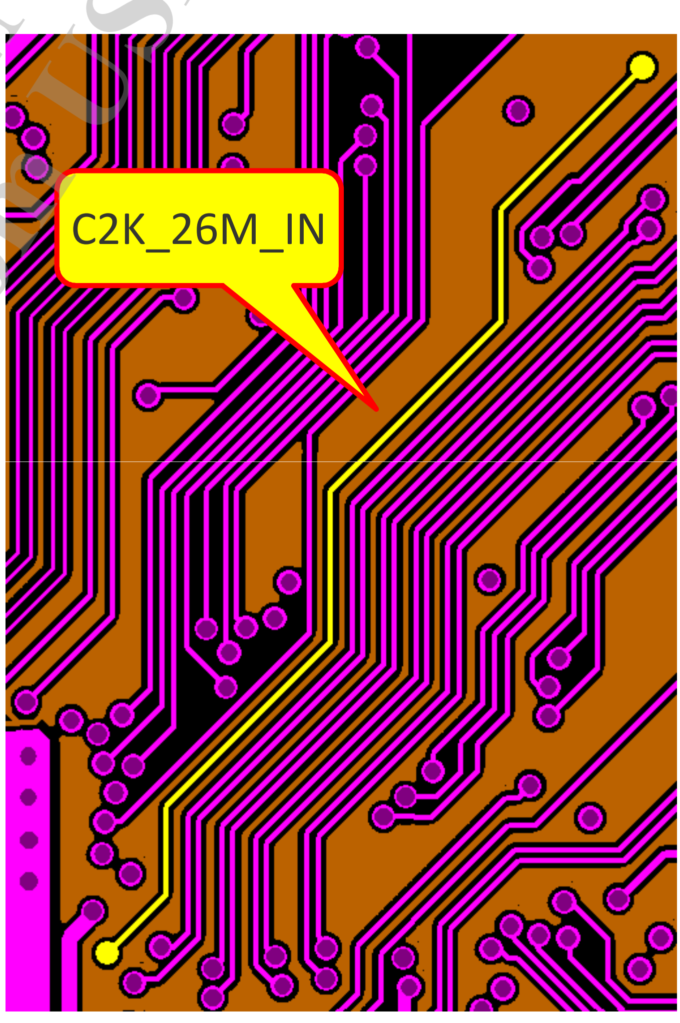


Fig.1

PCB Net Name	IC Ball Number
TX_BSI_EN	F9
TX_BSI_D0	G9
TX_BSI_CLK	F10
BSI_EN	E10
BSI_D0	J8
BSI_D0	K8



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MT6328
PCB Layout Guideline

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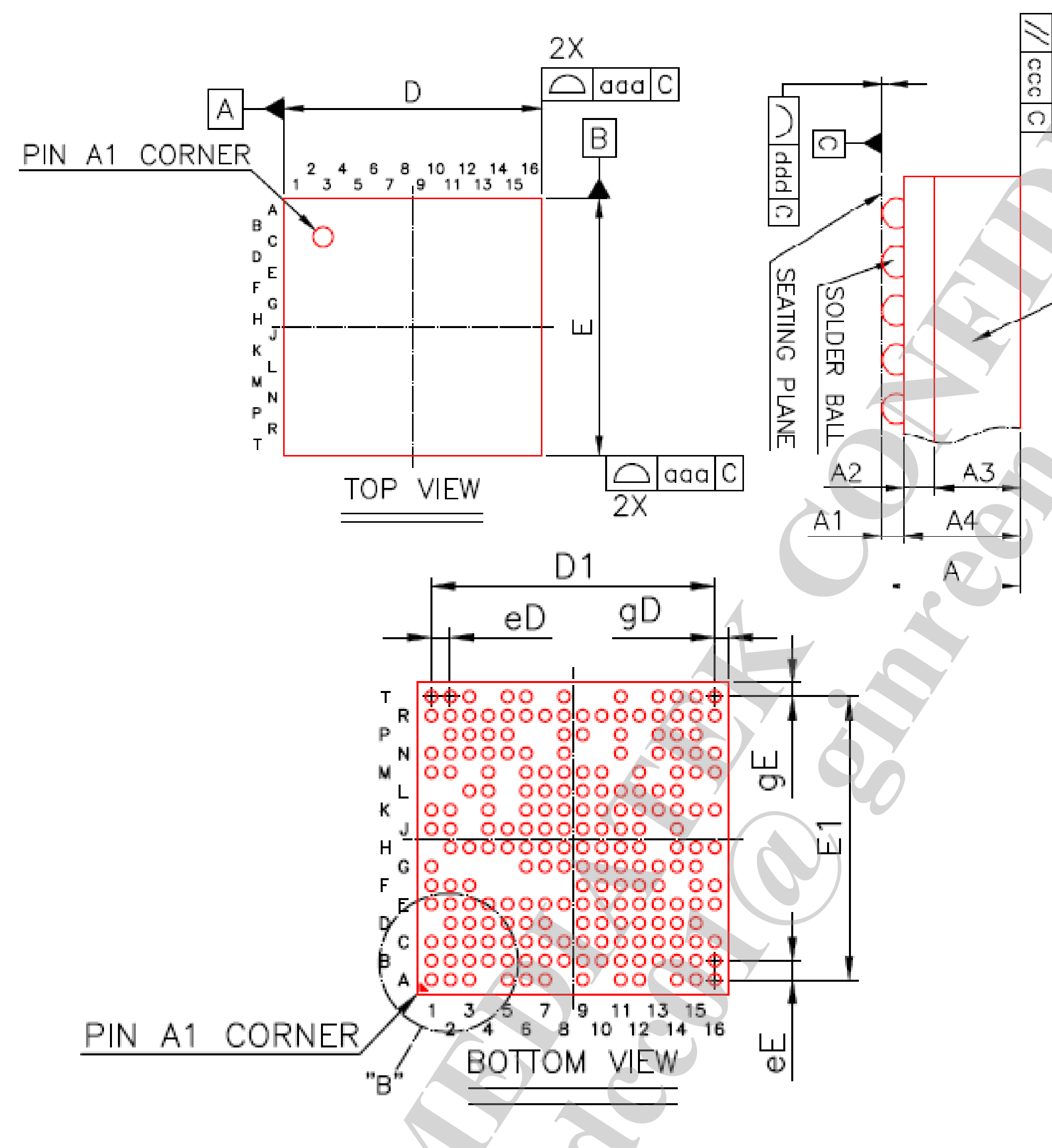
FOR dcc01@ginreen.com USE ONLY

Package outline of MT6328



Item		Symbol	Common Dimensions MIN.	NOM.	MAX.
Package Type				VFBGA	
Body Size	X	D	6.50	6.60	6.70
	Y	E	6.50	6.60	6.70
Ball Pitch	X	eD		0.40	
	Y	eE		0.40	
Mold Thickness		A3		0.65 Ref.	
Substrate Thickness		A2		0.11 Ref.	
Substrate+Mold Thickness		A4	0.71	0.76	0.81
Total Thickness		A	–	–	1.00
Ball Diameter				0.25	
Ball Stand Off		A1	0.12	0.16	0.20
Ball Width		b	0.20	0.25	0.30
Package Edge Tolerance		aaa		0.05	
Mold Flatness		ccc		0.10	
Coplanarity		ddd		0.08	
Ball Offset (Package)		eee		0.15	
Ball Offset (Ball)		fff		0.05	
Ball Count		n		206	
Edge Ball Center to Center	X	D1		6.00	
	Y	E1		6.00	
Edge Ball Center to Package Edge	X	gD		0.30	
	Y	gE		0.30	

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MT6328 Ball Map

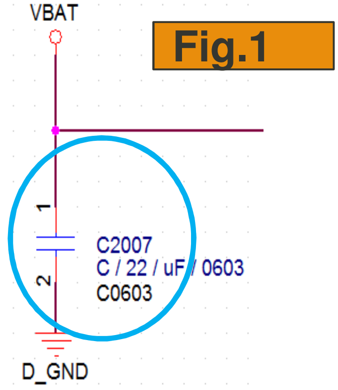
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	
A	AVDD45_VSYS22	VSYS22	AVSS45_VSYS22		VCORE1	VCORE1	VPROC		AVSS45_VPROC		AVDD45_VPROC	VLTE		AVSS45_VPA	VPA	AVDD45_VPA	A
B	AVDD45_VSYS22	VSYS22	AVSS45_VSYS22	AVDD45_VCORE1	VCORE1	AVSS45_VCORE1	VPROC	VPROC	AVSS45_VPROC	AVDD45_VPROC	AVDD45_VPROC	VLTE	AVDD45_VLTE	VPA_FB	AVSS45_VPROC_FB	AVSS45_SMPS	B
C	AVSS45_VCORE1_FB	VCORE1_FB	VSYS22_FB	AVDD45_VCORE1	AVDD45_VCORE1	AVSS45_VCORE1	VPROC	AVSS45_VPROC	AVSS45_VPROC	AVDD45_VPROC	AVSS45_VLTE	VLTE	AVDD45_VLTE	VLTE_FB	AVDD45_SMPS	VPROC_FB	C
D		EXT_PMIC_EN	RESETB	PMU_TESTMODE	AVSS45_LDO	AVSS45_VCORE1	VPROC		AVSS45_VPROC	AVDD45_VPROC	AVSS45_VLTE	AVSS45_VLTE	AVDD45_VLTE	AVDD45_SPK	CS_P		D
E	AVDD22_LDO2	PWRKEY	VCAMIO	VSRAM	AVSS45_LDO	AVSS45_LDO	AVSS45_LDO	AVSS45_LDO	AVSS45_LDO	AVSS45_LDO	AVSS45_LDO	AVSS45_LDO	AVSS45_VLTE_FB	AVSS45_SPK	CS_N	SPK_N	E
F	AVDD22_LDO3	VIO18	VCN18						VRF18_1	VRF18_0	AVSS45_LDO	AVSS45_LDO	AVSS18N_AUD		AU_FLYN	SPK_P	F
G	AVDD22_LDO4					AVSS45_LDO	AVSS45_LDO	AVSS45_LDO	AVSS45_LDO	AVSS45_LDO	AVSS45_LDO	AVSS45_LDO	AVDD18_AUD	AVSS18_AUD	AU_FLYP		G
H		VCAMD	AVDD22_LDO1	VGP1	VCAMAF	AVSS45_LDO	AVSS45_LDO	AVSS45_LDO	AVSS45_LDO	AVSS45_LDO	AVSS45_LDO	AVSS45_LDO		AU_REFN	AU_HPL	AU_HPR	H
J	VM	AVDD22_LDO1		VIBR	FCHR_ENB	AVSS45_LDO	AVSS45_LDO	AVSS45_LDO	AVSS45_LDO	AVSS45_LDO	AVSS45_LDO	CLK26M		AU_HSN			J
K	AVDD45_LDO5	VIO28		VMC		SPI_CLK	AVSS45_LDO	AVSS45_LDO	AVSS45_LDO	AVSS45_LDO	AVSS45_LDO	AVSS28_AUD	AU_VIN1_P	AU_VIN2_P	AU_HSP	AVDD28_AUD	K
L			AVSS45_VREF	VREF		SPI_MOSI	AVSS45_LDO	AVSS45_LDO	AVSS45_LDO	AVSS45_LDO	AVSS45_LDO	AVSS45_LDO	AU_VIN1_N	AU_VIN2_N			L
M	CHG_DM	AVDD45_LDO3		VSYSSNS		SPI_CSN	WDTRSTB_IN	AUD_CLK	RTC32K_2V8	AUD_DAT_MISO		AVDD18_AUXADC		ACCDET	AU_VIN0_N	AU_VIN0_P	M
N	CHG_DP	UVLO_VTH	BATSNS	ISENSE	SPI_MISO	HOMEKEY		AUD_DAT_MOSI			VSIM2		AVSS18_AUXADC	AVSS45_ISINK	AU_MICBIAS1	AU_MICBIAS0	N
P		BATON	CHRLDO	FSOURCE	RTC32K_1V8_0			SRCLKEN_IN0	VTCXO_0		VUSB33		TREF	AUXADC_VIN	ISINK1		P
R	VCDT	VDRV	ENBB	RTC32K_1V8_1	SRCLKEN_IN1	XOUT	AVSS28_RTC	AVDD28_RTC	VMCH	VEMC_3V3	VSIM1	VCN33	VCN28	VAUD28	VAUX18	ISINK0	R
T	XOSC_EN	DVDD18_IO	DVDD18_DIG		DVSS18_IO	XIN		AVDD45_LDO2			AVDD45_LDO4		AVDD45_LDO1	VCAMA	VEFUSE	VTCXO_1	T
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	

Legend
Buck Output
LDO Output
Power Input
AUDIO
AUXADC
GND
32K Clock

MT6328 Power Input (1/2)

VSYS Input-

- 22uF capacitor (C2007) is placed near MT6328 **VSYS** input balls (Fig.1).
- To route from 22uF capacitor (C2007), use start topology to connect to each device.
  1. **VSYS** input for BUCK (Fig.2)
  2. **VSYS** input for LDO (Fig.3)
  3. **VSYS** power current (Fig.4)
- All the decoupling capacitors should be placed near MT6328. The priority is buck capacitor then decoupling capacitor of LDO (Fig.4).



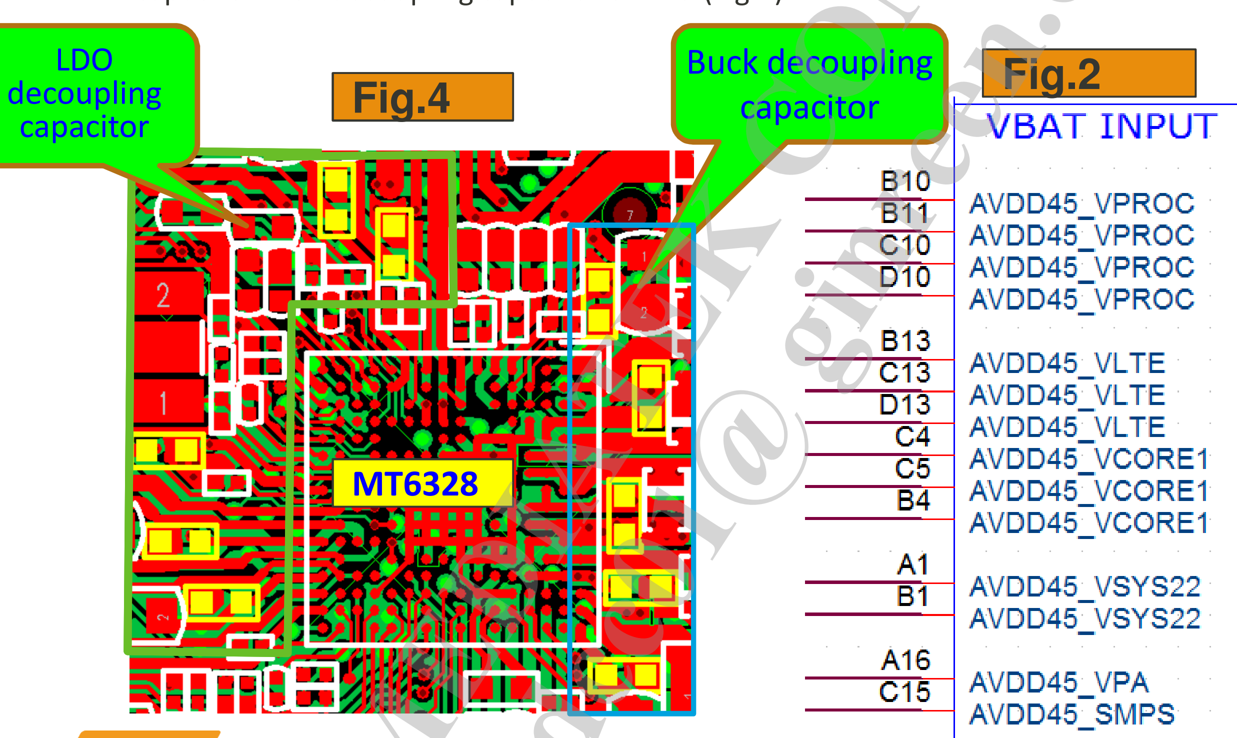


Fig.3

Ball	Net
T13	AVDD45_LDO1
T8	AVDD45_LDO2
K1	AVDD45_LDO3
T11	AVDD45_LDO4
M2	AVDD45_LDO5

Fig.4

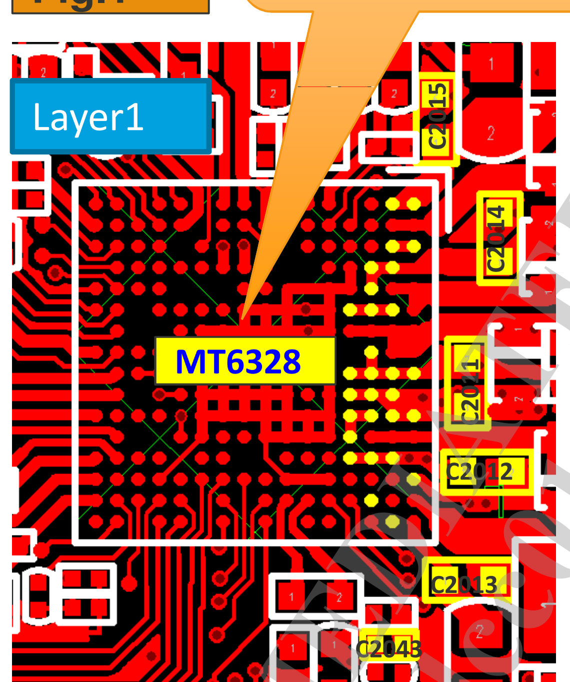
Power net	Current
AVDD45_VPROC	5A
AVDD45_VLTE	2.8A
AVDD45_VCORE1	3.5A
AVDD45_VSYS22	1.9A
AVDD45_VPA	600mA
AVDD45_SMPS	1mA
AVDD45_LDO1	810mA
AVDD45_LDO2	800mA
AVDD45_LDO3	400mA
AVDD45_LDO4	720mA
AVDD45_LDO5	500mA

MT6328 Power Input (2/2)

- **Layout method of MT6328 power input for Buck GND**
  - Buck GND balls are connected to buck capacitors (C2011~C2015, C2043) with planes or wide trace.
  - The GND pins of buck capacitors should be connected together and isolated from nearby GND trace and plane then connected to the main GND at L3 (Fig.1~Fig.3).

Fig.1

Use more vias to help thermal. At least 6-8 PTH visa and 25 laser vias.



Layer2: BUCK GND is isolated from nearby GND trace and plane.

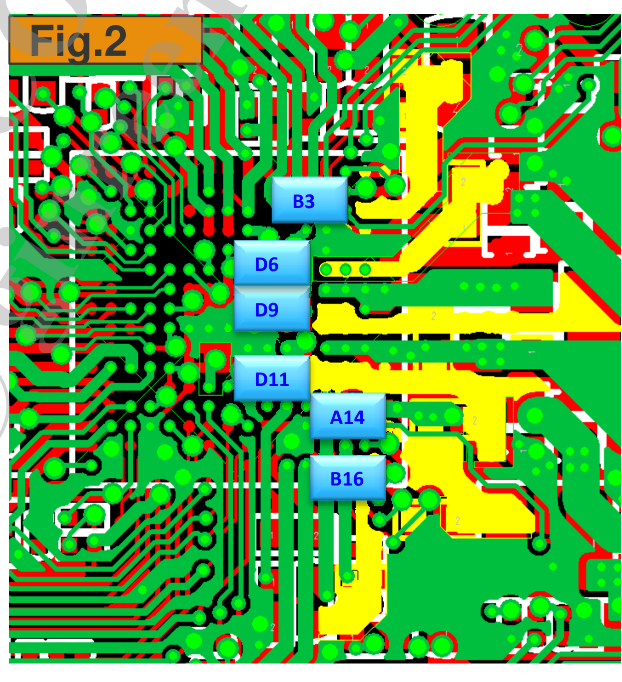


Fig.3

Pin	Net
A9	AVSS45_VPROC
B9	AVSS45_VPROC
C8	AVSS45_VPROC
C9	AVSS45_VPROC
D9	AVSS45_VPROC
B6	AVSS45_VCORE1
C6	AVSS45_VCORE1
D6	AVSS45_VCORE1
C11	AVSS45_VLTE
D11	AVSS45_VLTE
D12	AVSS45_VLTE
A3	AVSS45_VSYS22
B3	AVSS45_VSYS22
A14	AVSS45_VPA
B16	AVSS45_SMPS

MT6328 Buck Output (1/3)

- The buck inductors should be placed near MT6328 (Fig.1).
- The output current is shown in Fig.2.

Fig.1

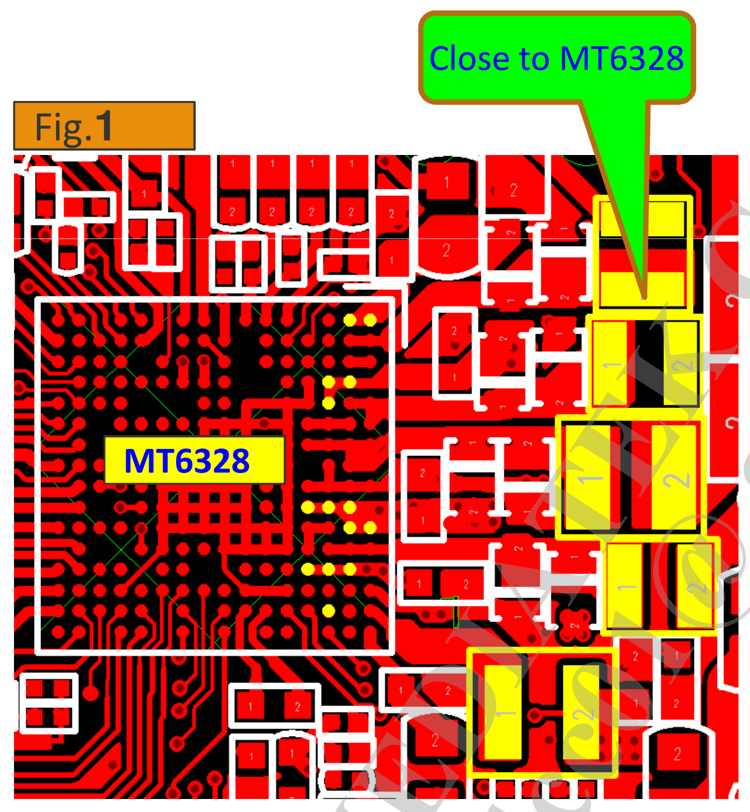


Fig.2

Output ball name	Output current (mA)
VPROC	5000
VLTE	2800
VCORE1	3500
VSYS22	1900
VPA	600

BUCK OUTPUT

Signal	Ball
VPROC	A7
VPROC	B7
VPROC	C7
VPROC	D7
VPROC	B8
VPROC_FB	C16
AVSS45_VPROC_FB	B15
VLTE	A12
VLTE	B12
VLTE	C12
VLTE_FB	C14
AVSS45_VLTE_FB	E13
VCORE1	A5
VCORE1	A6
VCORE1	B5
VCORE1_FB	C2
AVSS45_VCORE1_FB	C1
VSYS22	A2
VSYS22	B2
VSYS22_FB	C3
VPA	A15
VPA_FB	B14

MT6328 Buck Output (2/3)

- VPROC_PMIC_FB_6328/GND_VPROC_FB_6328

  VLTE_PMIC_FB/GND_VLTE_FB

  VCORE_PMIC_FB/GND_VCORE_FB

- Those signals are differential pairs and should be shielded by GND and far away from noise signals (Fig.1).

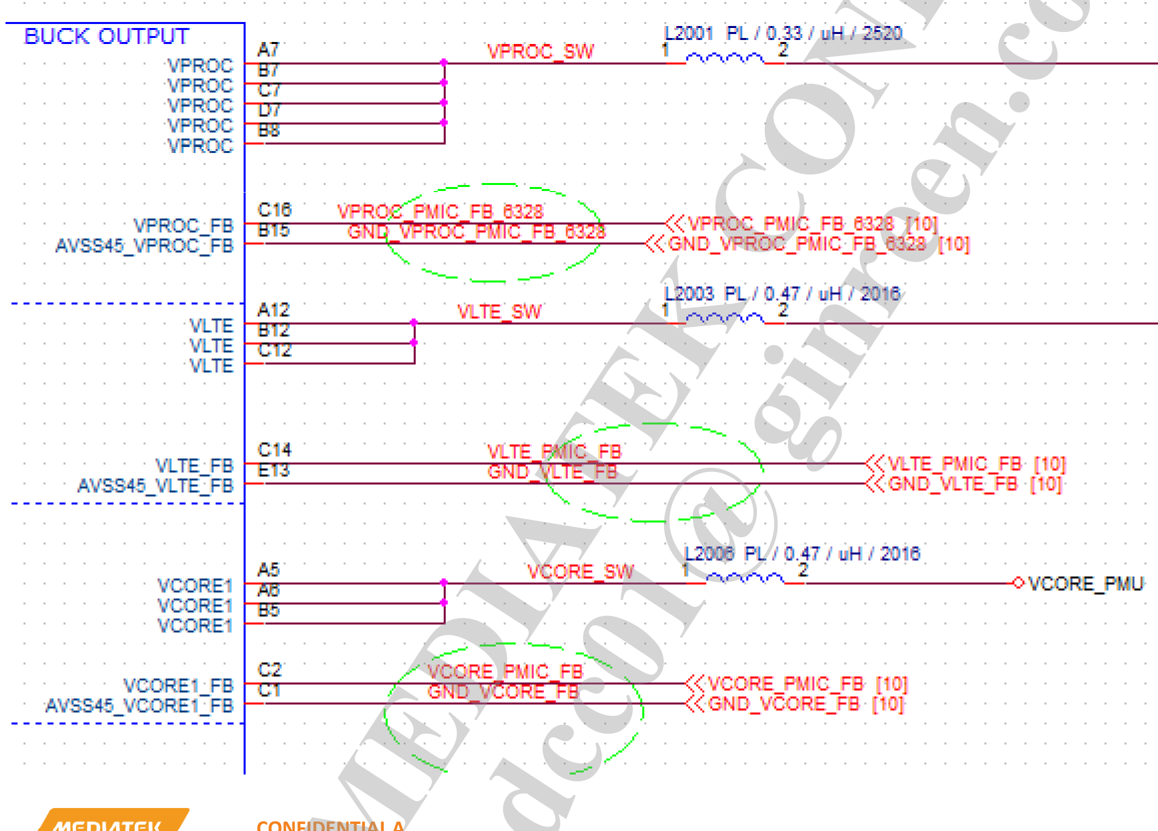
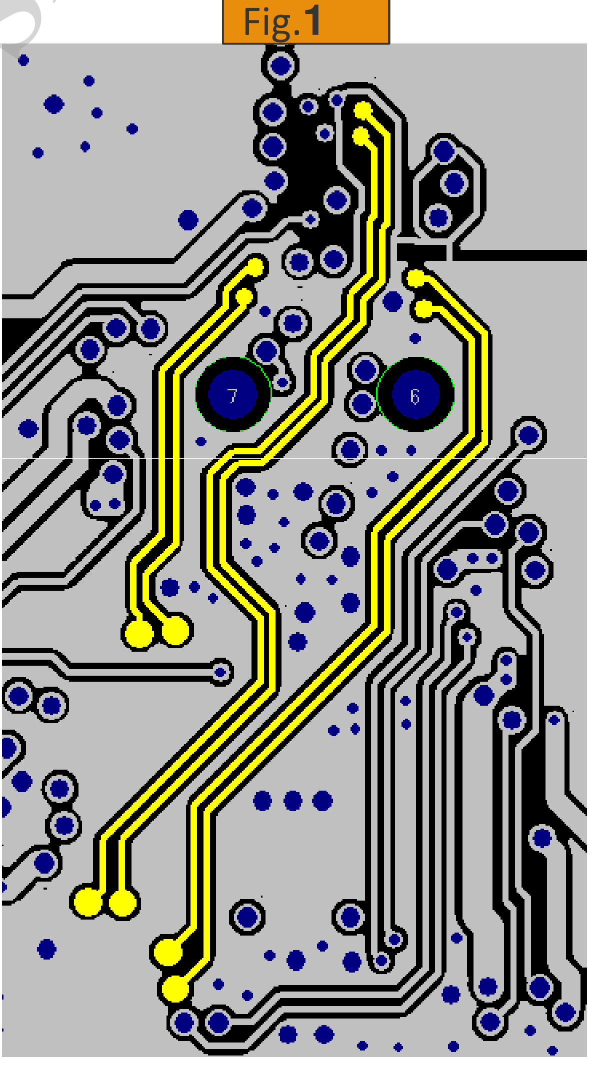


Fig.1



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MT6328 Buck Output (3/3)

- For VSYS22_FB and VPA_FB trace width=4mil, connect to output bypass capacitors directly and far away from noise signals (Fig.1~Fig.3).

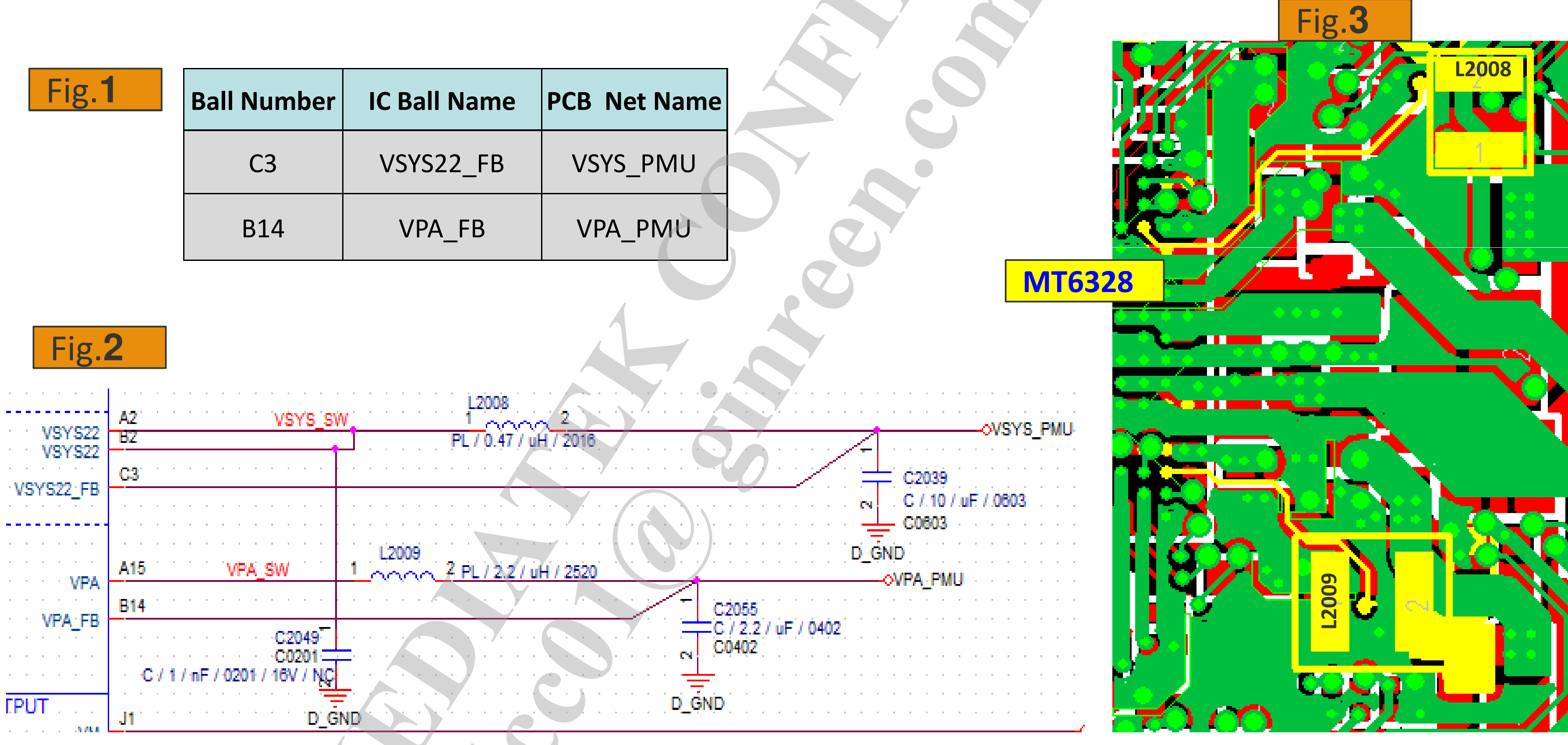

Fig.1

Ball Number	IC Ball Name	PCB Net Name
C3	VSYS22_FB	VSYS_PMU
B14	VPA_FB	VPA_PMU

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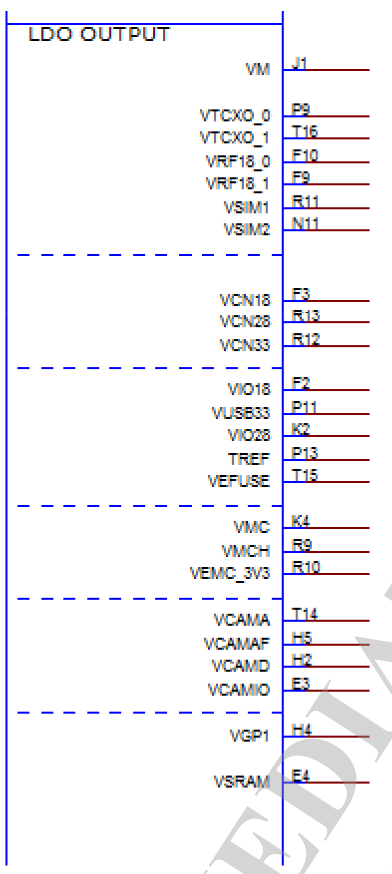
MT6328 LDO Output (1/2)

- LDO output layout suggestion is shown in Fig.1



LDO output layout suggestion

Layout Constraint for stability

(Fig.1)

Calculation PCB ESR is from PMIC LDO output ball to bypass cap
******************Excluded PCB IR drop******************

Type	PCB ESR	PCB Length/width
Special LDO: VM and VSRAM	ESR≦60mΩ	L/W=1500mil/18mil
Other LDOs	ESR≦200mΩ	L/W=2800mil/8mil

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MT6328 LDO Output (2/2)

- VREF capacitor (C2030) should be placed near L4/L3 pin.
- Capacitor C2031/C2057 should be placed near T2/T3 pin.

C2031/C2057/C2030 close to MT6328

R2042 R / 0 / ohm / 0402 R0402

C2031 C / 100 / nF / 0201 C0201

C2057 C / 1 / uF / 0201 C0201

C2030 C / 100 / nF / 0201 C0201

D_GND

Close to MT6328

DIG Power
T2 DVDD18_IO
T3 DVDD18_DIG
T5 DVSS18_IO
VREF
L4 VREF
L3 AVSS45_VREF
GND
A9 AVSS45_VPROC
B9 AVSS45_VPROC
C8 AVSS45_VPROC
C9 AVSS45_VPROC

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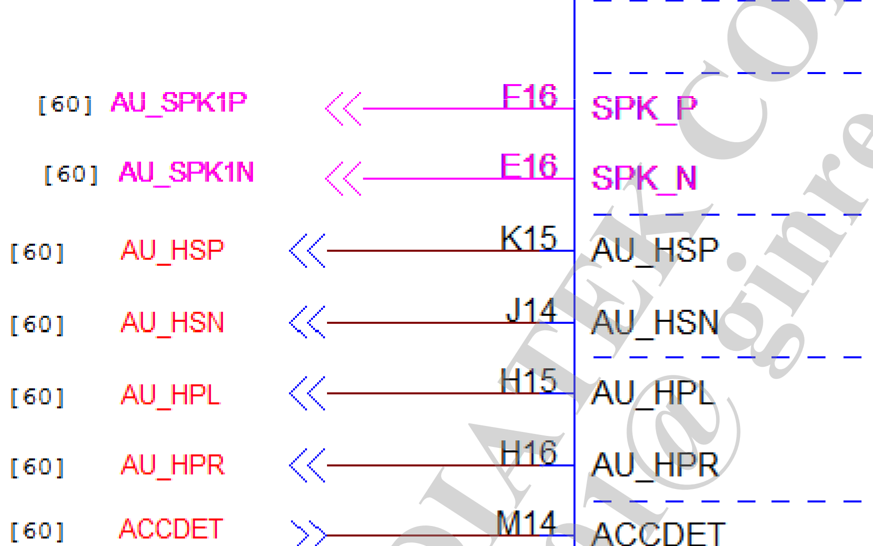
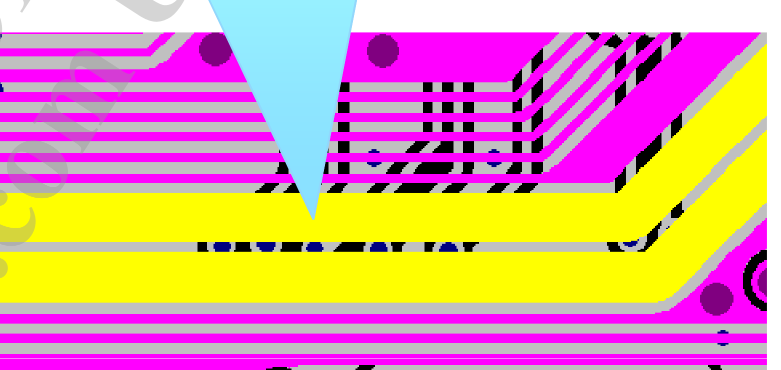
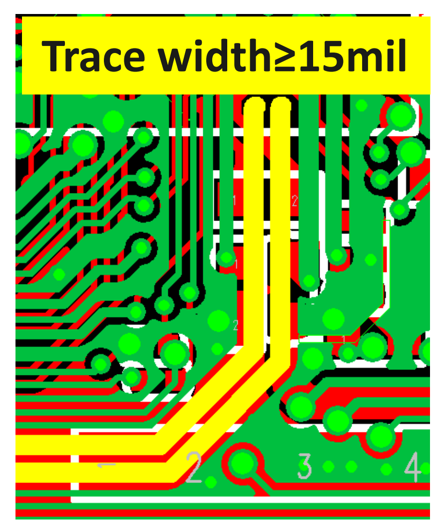
MT6328 Speaker

- Speaker signals should be shielded with GND (isolated with GND around the signal) and trace width ≧15mil.
- Speaker signals should be routed orthogonally to other signals between adjacent layers.







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MT6328 Audio

- These signals in Table 1 should be routed as differential pairs and shielded by GND (adjacent and up/down layers).
- Other signals should be routed orthogonally to other signals between adjacent layers.
- AU_HPR/AU_HPL signals should be shielded by GND respectively.
- Related capacitors should be placed near MT6328 (Fig.1~Fig.4).

Table 1

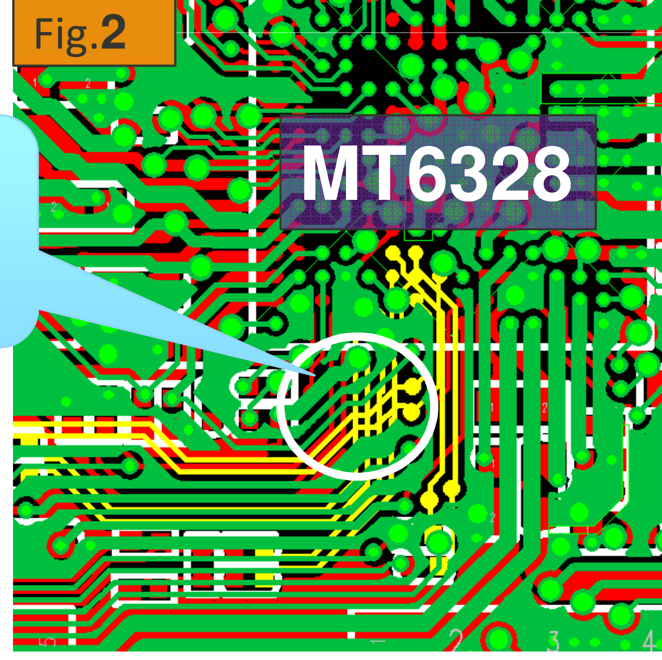
Ball Number	PCB Net Name	IC Ball Name
M16	AU_VIN0_P	AU_VIN0_P
M15	AU_VIN0_N	AU_VIN0_N
K13	AU_VIN1_P	AU_VIN1_P
L13	AU_VIN1_N	AU_VIN1_N
K14	AU_VIN2_P	AU_VIN2_P
L14	AU_VIN2_N	AU_VIN2_N
J14	AU_HSN	AU_HSN
K15	AU_HSP	AU_HSP
H16	**AU_HPR**	**AU_HPR**
H15	**AU_HPL**	**AU_HPL**

Fig.1

MT6328

Diff. Pairs

Routed orthogonally to other signals between adjacent layers.



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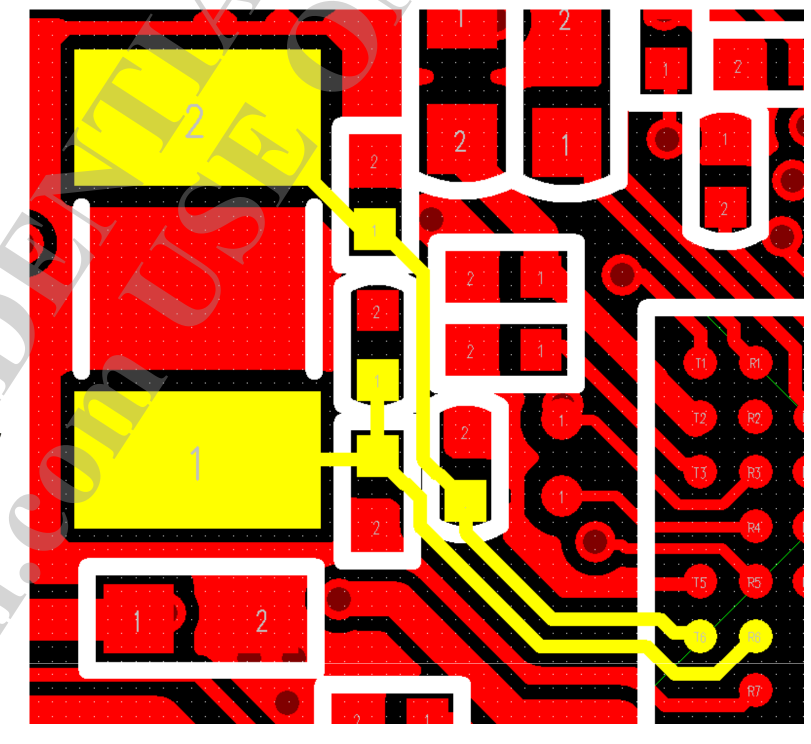
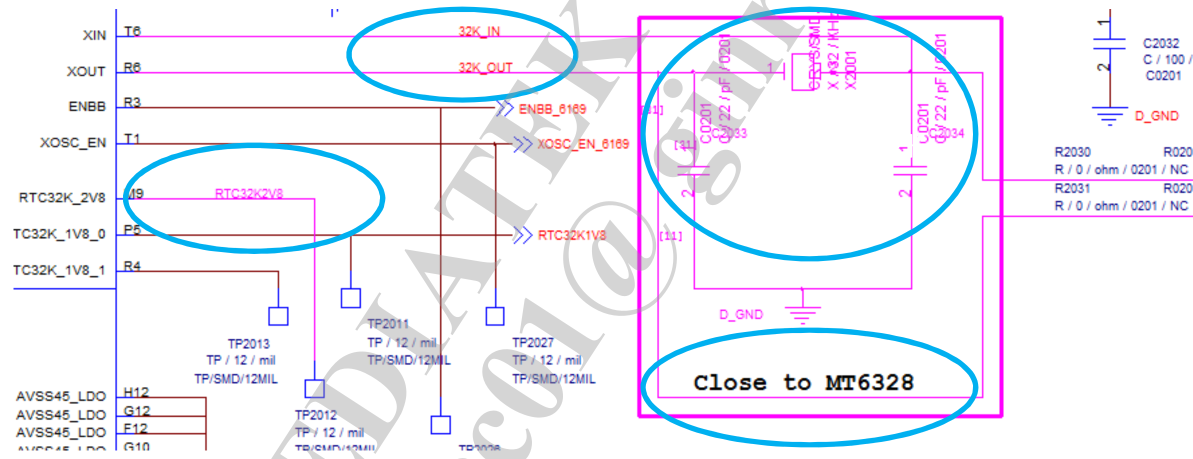
MT6328 32K Crystal



32K Crystal-

- 32K crystal and related parts should be placed close to MT6328.
- 32K_IN and 32K_OUT should be shielded by GND (adjacent and up/down layers).
- RTC32K1V8 should be shielded by GND (adjacent and up/down layers).



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MT6328 Others (1/2)

Charger-

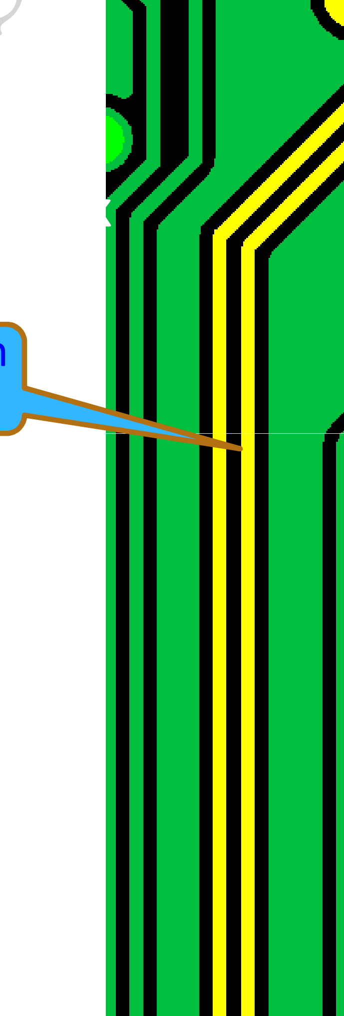
- BATSNS/ISENSE (ball: N3/N4) should be routed as differential pairs and far away from noise signals.

Diff. pairs

4 mil trace with good shielding (Differential)

BATSNS
ISENSE
R2043 R / 0 / ohm / 0402 R0402
R2044 R / 0 / ohm / 0402 R0402
C2054
C / 100 / nF / 0201
C0201
D_GND
TP2017
TP / 12 / mil
TP/SMD/12MIL
U2001-C
Charger
J5 FCHR_ENB
N3 BATSNS
N4 ISENSE
M4 VSYSSNS
P2 BATON
VBAT
VBUS
R2045
R / 0 / ohm / 0402
C2051
C / 1 / uF / 0201
C0201
R0402
BAT_ON
330 / K / 0402 / 1%
R2032

Far away from noise signals



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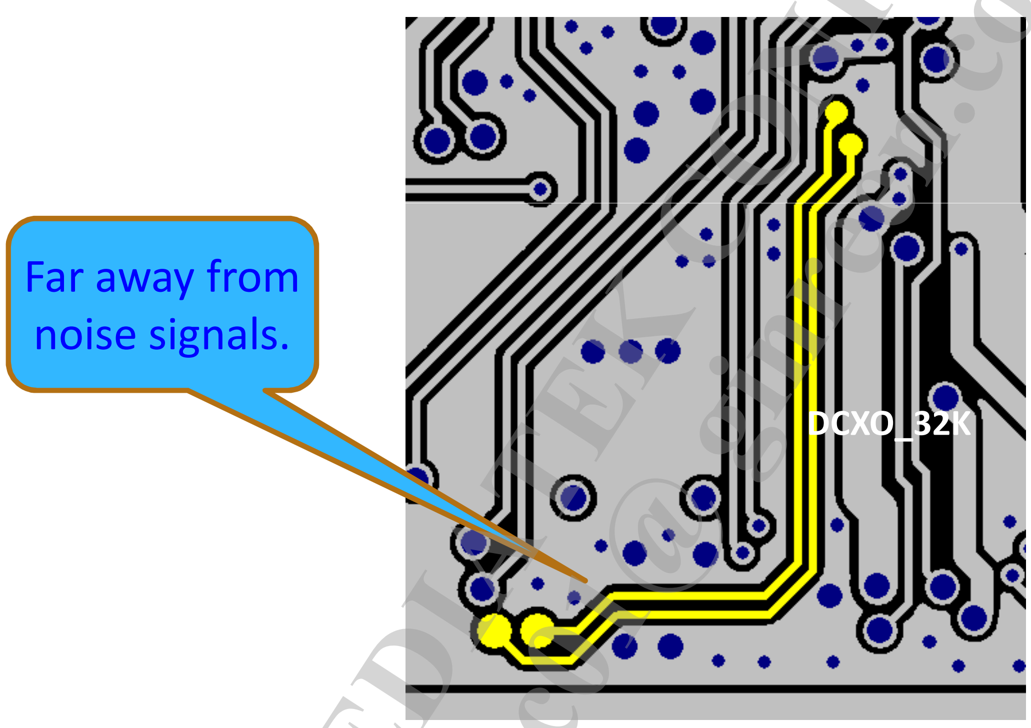
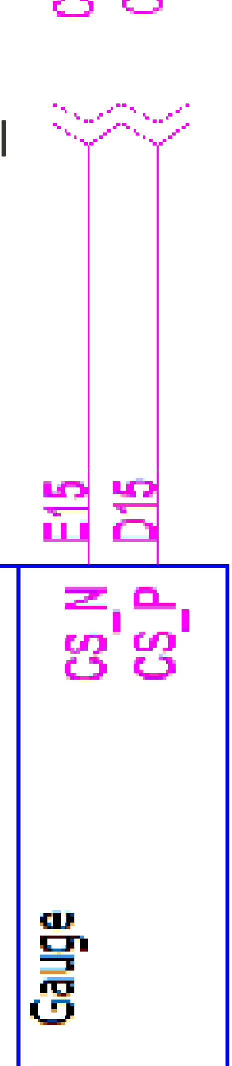
MT6328 Others (2/2)

Gauge-

- CS_N/CS_P (ball: E19/D19) should be routed as differential pairs and far away from noise signals.





Outlines

- **Brief Introduction to MT6737**
- **Packaging**
  - Package Outline of MT6737
  - MT6737 Footprint Recommendation
  - MT6737 Ball Out Design
- **General Guidelines**
  - PCB Stack-up Recommendation
  - Common Rules and Via Type
  - Placement Notes
  - MT6737 Fan Out
- **Design Guidelines for High-Speed Digital Signals**
  - LPDDR3
  - LPDDR2
  - PDN Design
- **Others**
  - MT6737 RF Interface - MT6169 - MT6158
  - MT6328 (PMU)
  - MT6625 (BT/FM/WiFi/GPS)
  - USB/MIPI/SIM Card/T-Card/eMMC/Differential Pair Layout Suggestion

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MT6625
PCB Layout Guideline

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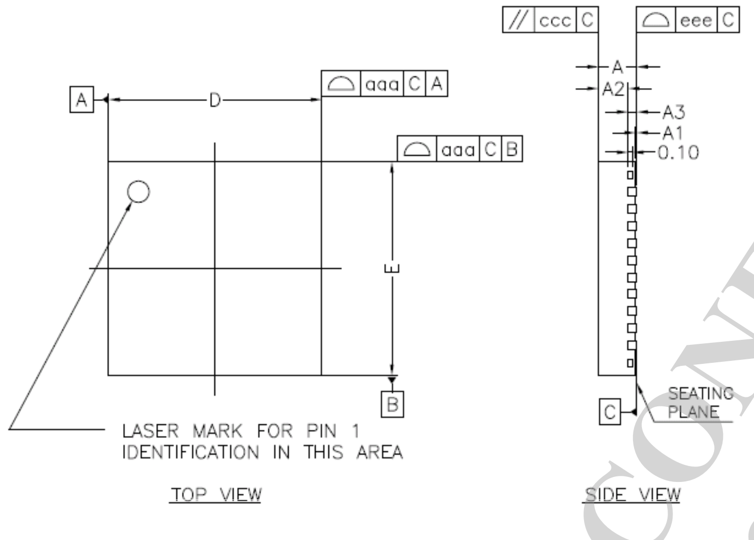
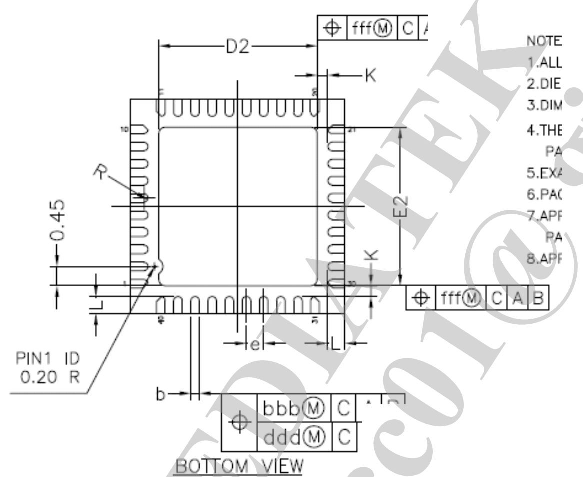
Package Outline of MT6625





* CONTROLLING DIMENSION : MM

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.80	0.85	0.90	0.031	0.033	0.035
A1	0.00	---	0.05	0.00	---	0.002
A2	---	0.65	0.70	---	0.026	0.028
A3	0.20 REF.			0.008 REF.		
b	0.15	0.20	0.25	0.006	0.008	0.010
D	5.00 bsc			0.197 bsc		
D2	3.60	3.70	3.80	0.142	0.146	0.150
E	5.00 bsc			0.197 bsc		
E2	3.60	3.70	3.80	0.142	0.146	0.150
L	0.35	0.40	0.45	0.014	0.016	0.018
e	0.40 bsc			0.016 bsc		
R	0.075	---	---	0.003	---	---
K	0.20	---	---	0.008	---	---
TOLERANCES OF FORM AND POSITION						
aaa	0.10			0.004		
bbb	0.07			0.003		
ccc	0.08			0.003		
ddd	0.05			0.002		
eee	0.08			0.003		
fff	0.10			0.004		

NOTES :

1.ALL DIMENSIONS ARE IN MILLIMETERS.

2.DIE THICKNESS ALLOWABLE IS 0.305 mm MAXIMUM(.012 INCHES MAXIMUM)

3.DIMENSIONING & TOLERANCES CONFORM TO ASME Y14.5M. −1994.

4.THE PIN #1 IDENTIFIER MUST BE PLACED ON THE TOP SURFACE OF THE PACKAGE BY USING INDENTATION MARK OR OTHER FEATURE OF PACKAGE BODY.

5.EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.

6.PACKAGE WARPAGE MAX 0.08 mm.

7.APPLIED FOR EXPOSED PAD AND TERMINALS. EXCLUDE EMBEDDING PART OF EXPOSED PAD FROM MEASURING.

8.APPLIED ONLY TO TERMINALS.

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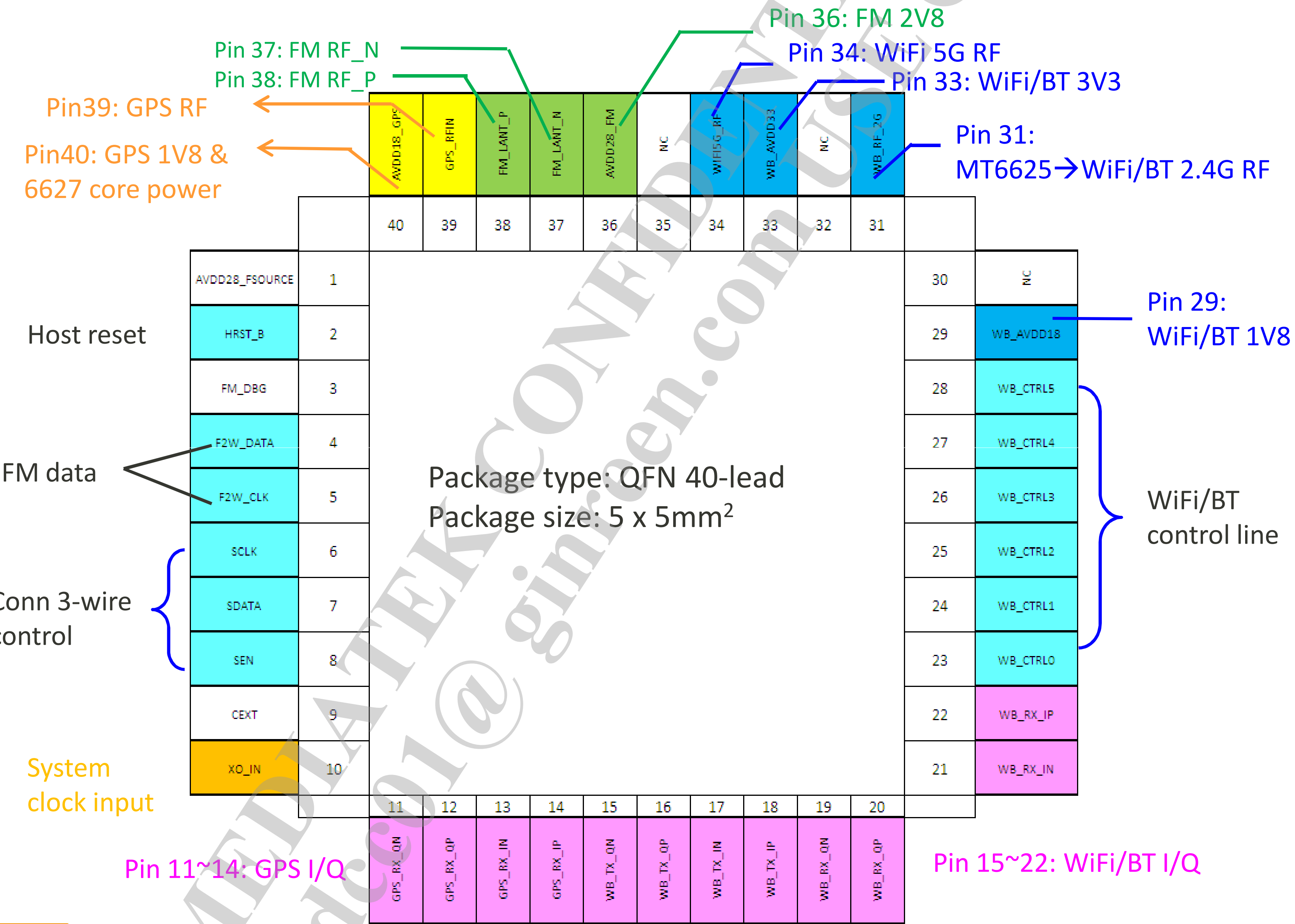
MT6625 Pin Definition



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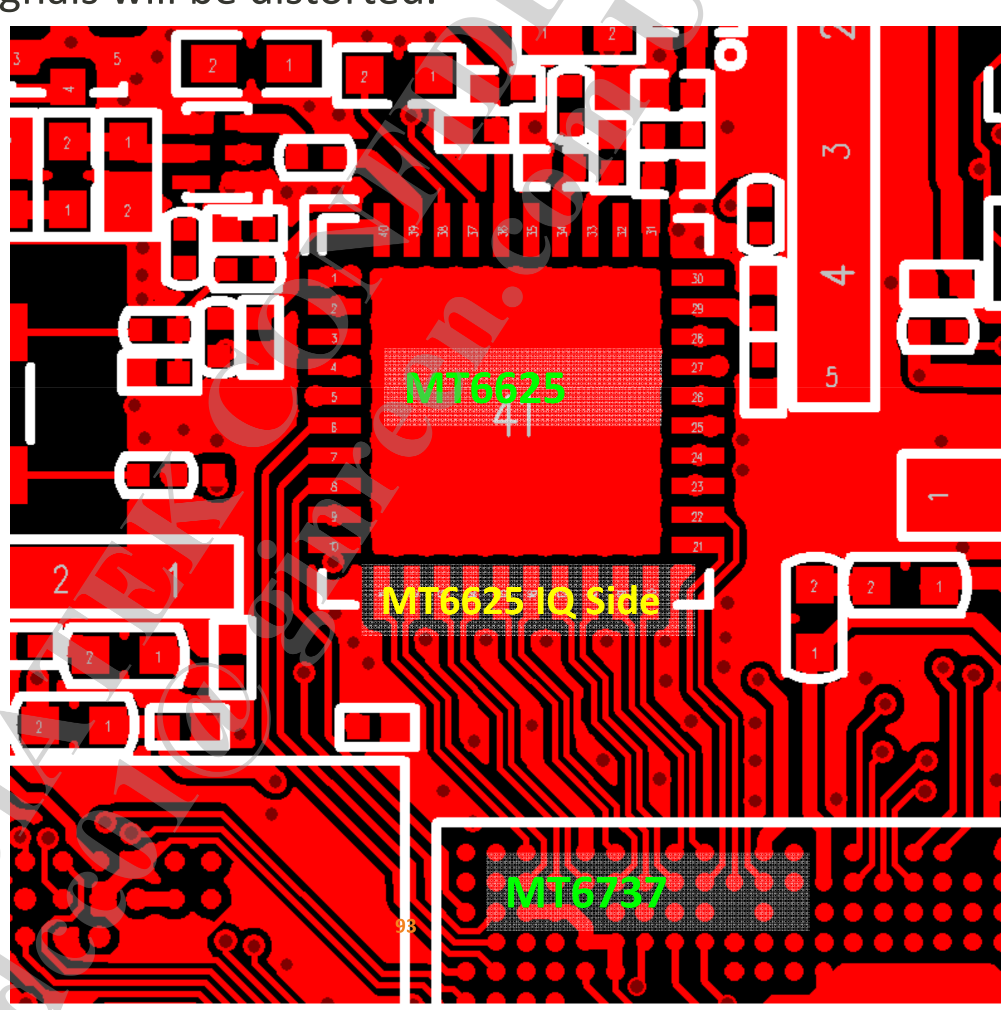
MT6625 v.s. MT6737 Placement

- Keep the distance between MT6625 and MT6737 among 0.2cm~5cm.
  - If < 0.2cm: Will weaken the sensitivity of microwave circuit transmission.
  - If > 5cm: IQ signals will be distorted.



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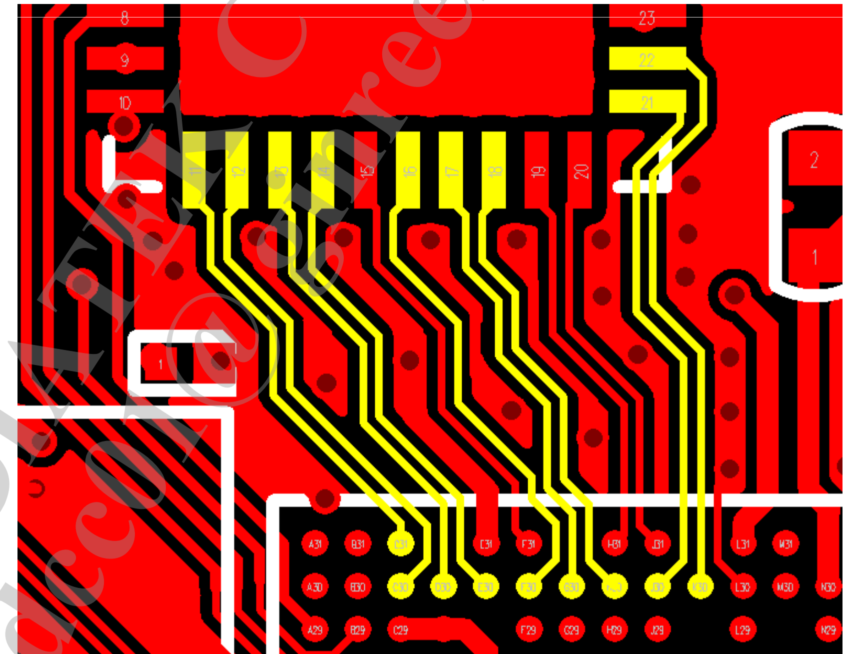
MT6625 IQ Trace

- IQ signals are differential pairs. Every pair must be shielded by GND (adjacent & up/down layers).

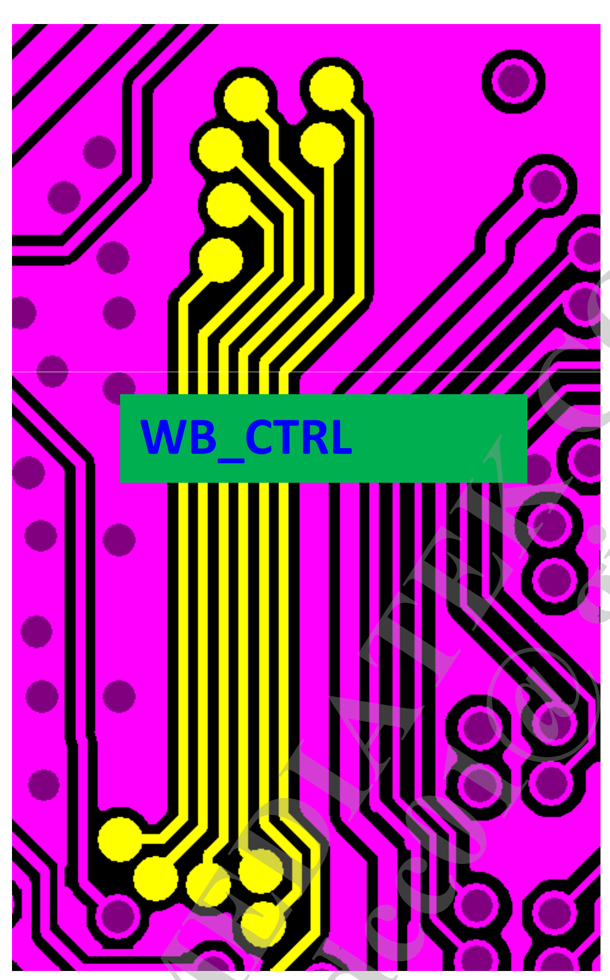
  If the layout area is not enough, you can simply shield the TX/RX groups. For example,
  RX group: WB_RX_IP/IN/QP/QN Pin19~Pin22
  TX group: WB_TX_IP/IN/QP/QN Pin 15~Pin18
  GPS RX group: GPS_RX_IP/IN/QP/QN Pin11~Pin14

- IQ trace total length ≦5cm



MT6625 WB Control Trace

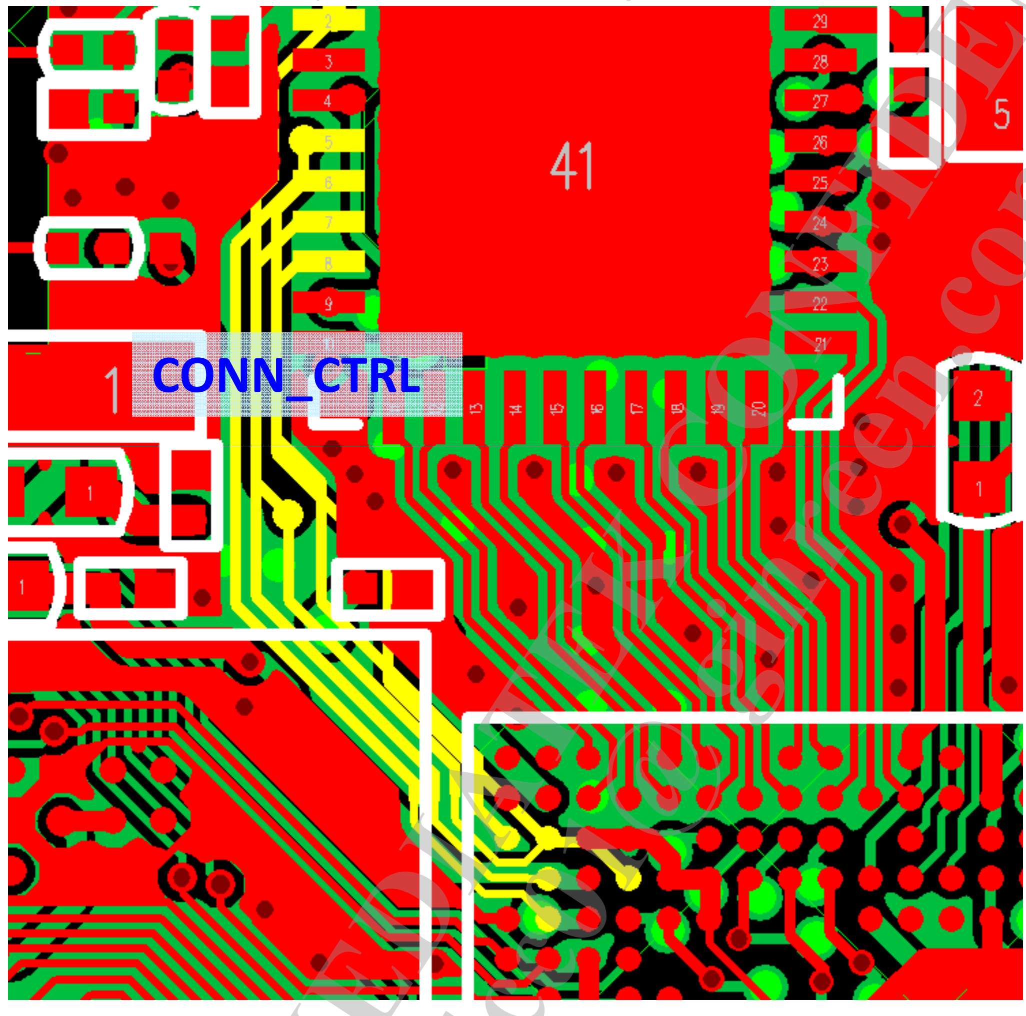
- Do not overlap with power and IQ signals.
- Keep WB_CTRL group together and shielded by GND.



Group	PCB Net-name
WB_CTRL	WB_CTRL0
	WB_CTRL1
	WB_CTRL2
	WB_CTRL3
	WB_CTRL4
	WB_CTRL5

MT6625 Other Control Traces

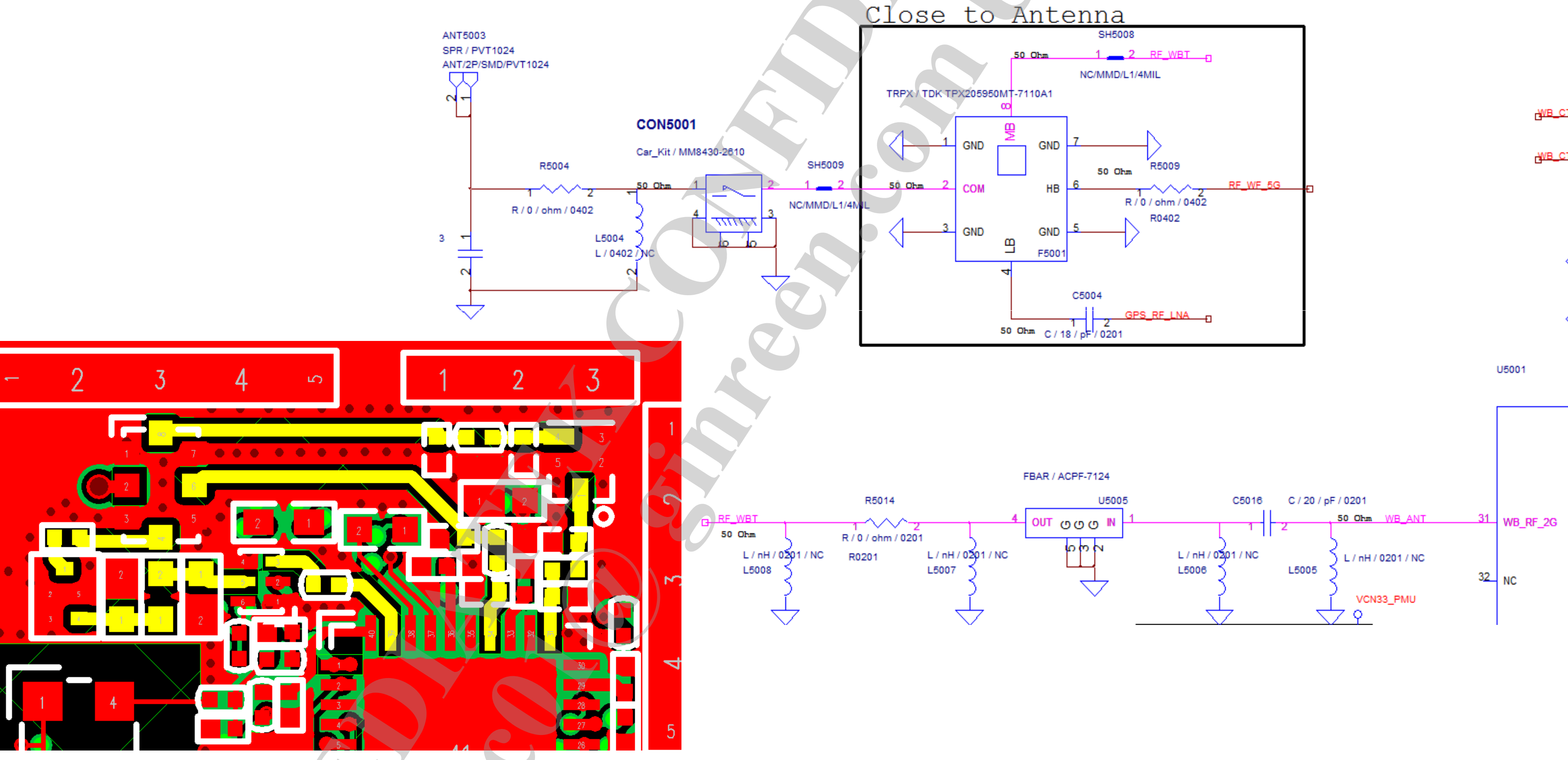
- Use only two layers (L2/L4) for CONN_CTRL group as you can and do not overlap them with power and IQ signals.



Group	PCB Net-name
CONN_CTRL	CONN_SEN
	CONN_SDATA
	CONN_SCLK
	CONN_RSTB
	F2W_CLK
	F2W_DATA

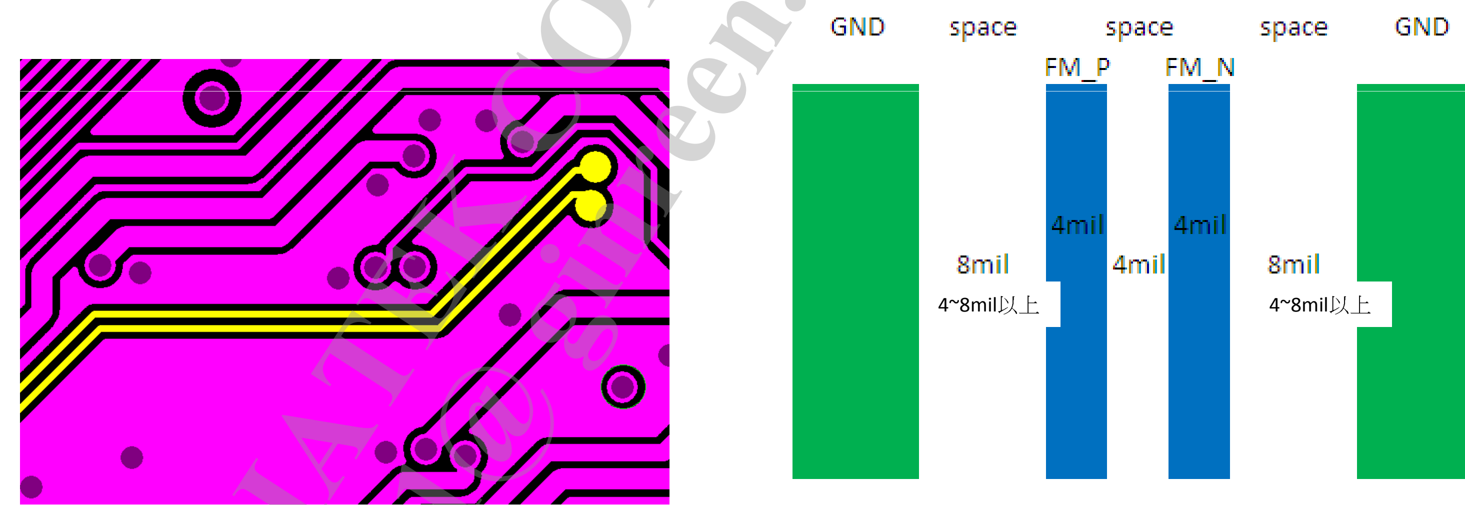
RF Trace - WiFi/BT/GPS

- Pin31 is the antenna pin for WiFi /BT/GPS.
- Keep 50Ω impedance well shielded by GND (adjacent and up/down layers) and far away from digital signals.



RF Trace - FM

- FM signals are required for differential pairs to get better noise immunity.
- Plan FM routing path at the beginning, and FM signals must be shielded by GND with stitching GND via.
- If RF trace cannot be protected well, it will easily make noise to FM.
- It can avoid ESD interference if FM trace is in the inner layer and has good GND shielding.



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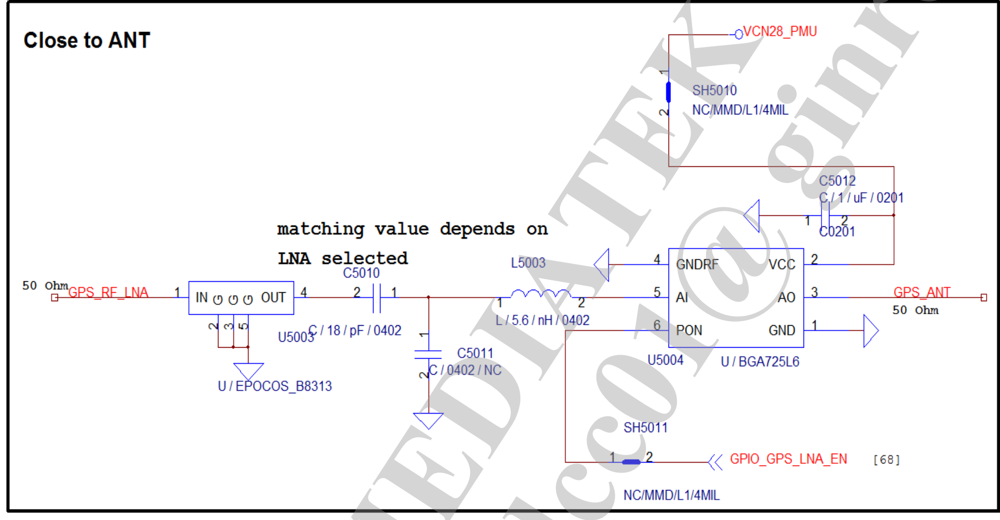
GPS Ext. LNA Placement

- GPS's LNA should be close to antenna and keep 50Ω impedance.

close to antenna

GPS xLNA



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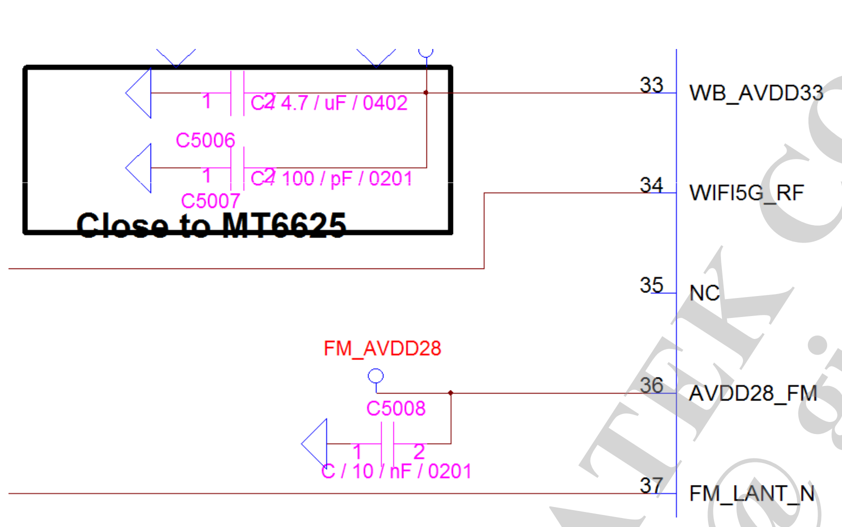
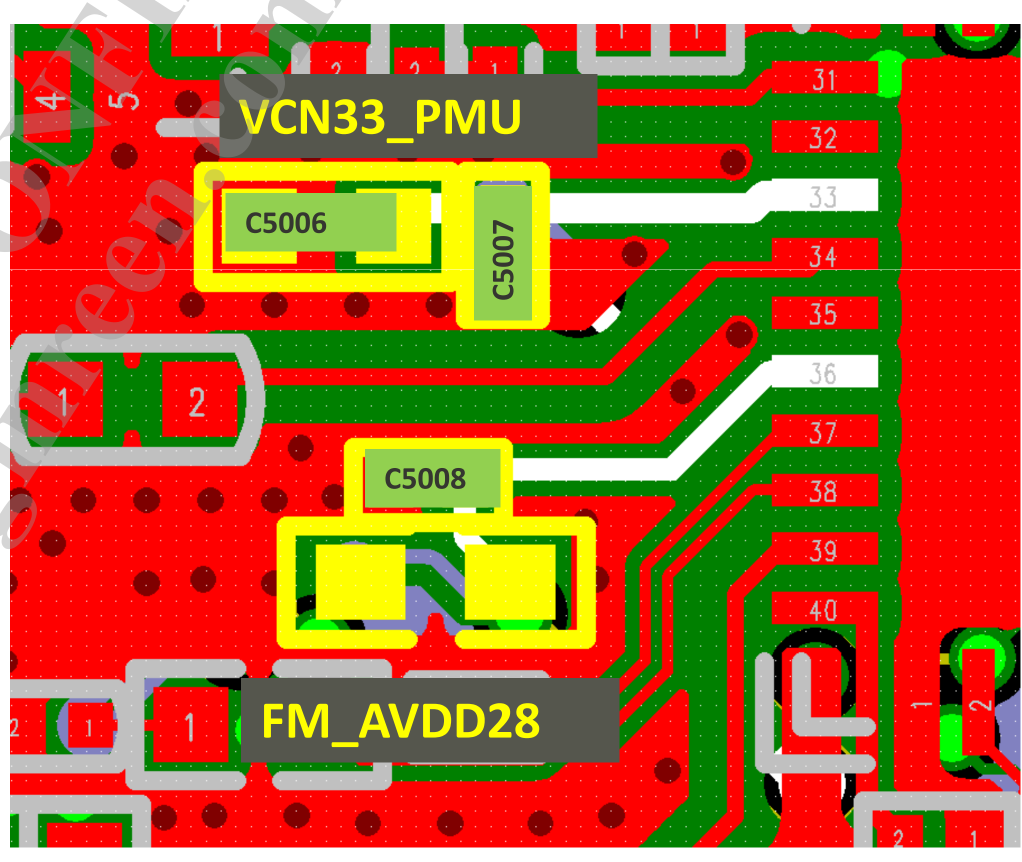
Power Trace (1/2)

- VCN33_PMU: Max. current is 200mA; place decupling capacitors close to power pin.
- FM_AVDD28: Max. current is 30mA; place decupling capacitors close to power pin.





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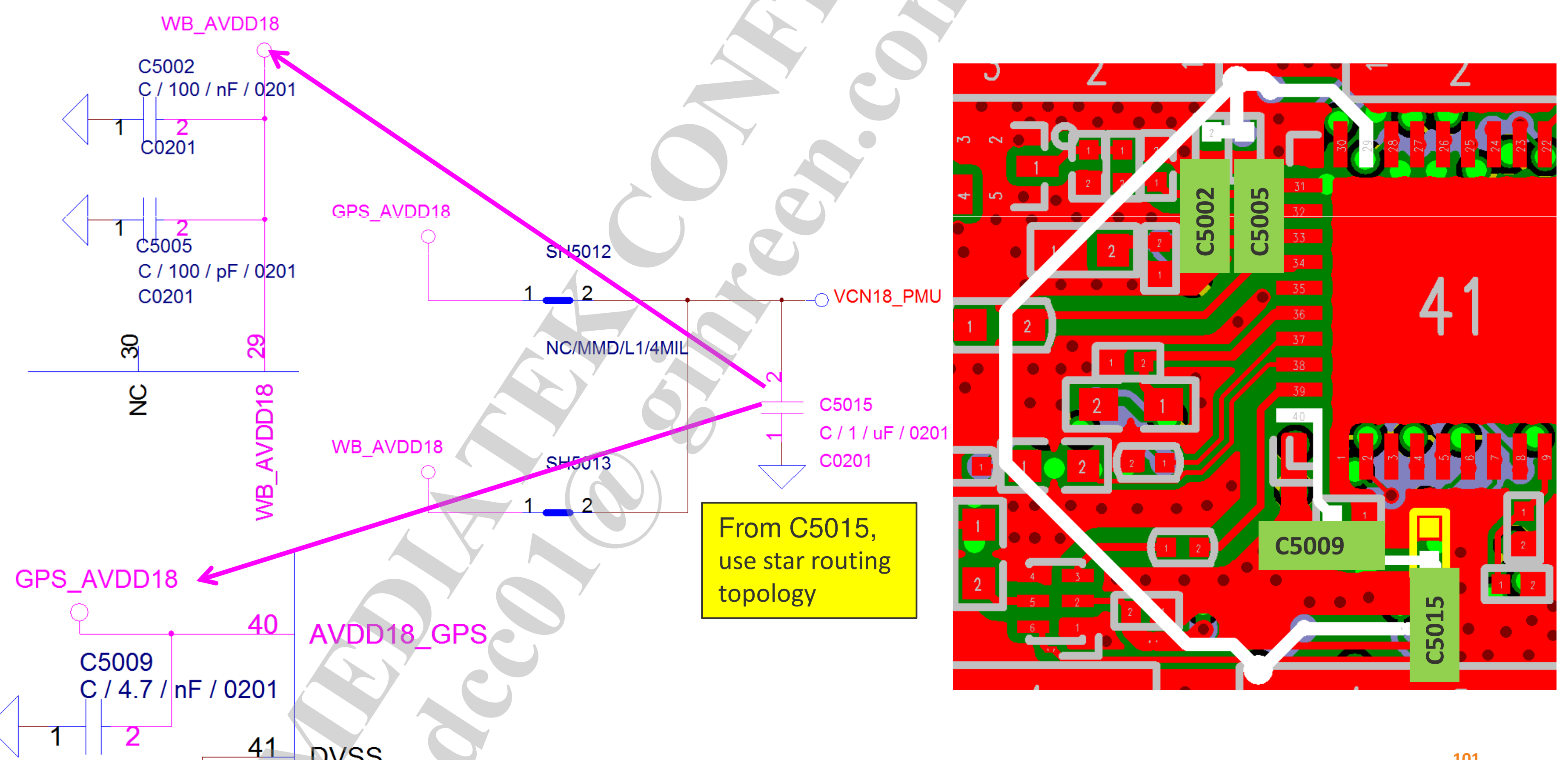
Power Trace (2/2)

- WB_AVDD18: Max. current is 50mA; place decupling capacitors close to power pin.
- GPS_AVDD18: Max. current is 20mA; place decupling capacitors close to power pin.
- Power trace VCN18_PMU is started from bypass capacitor (C5015/1uF) and uses star routing topology to connect to WB_AVDD18 and GPS_AVDD18.



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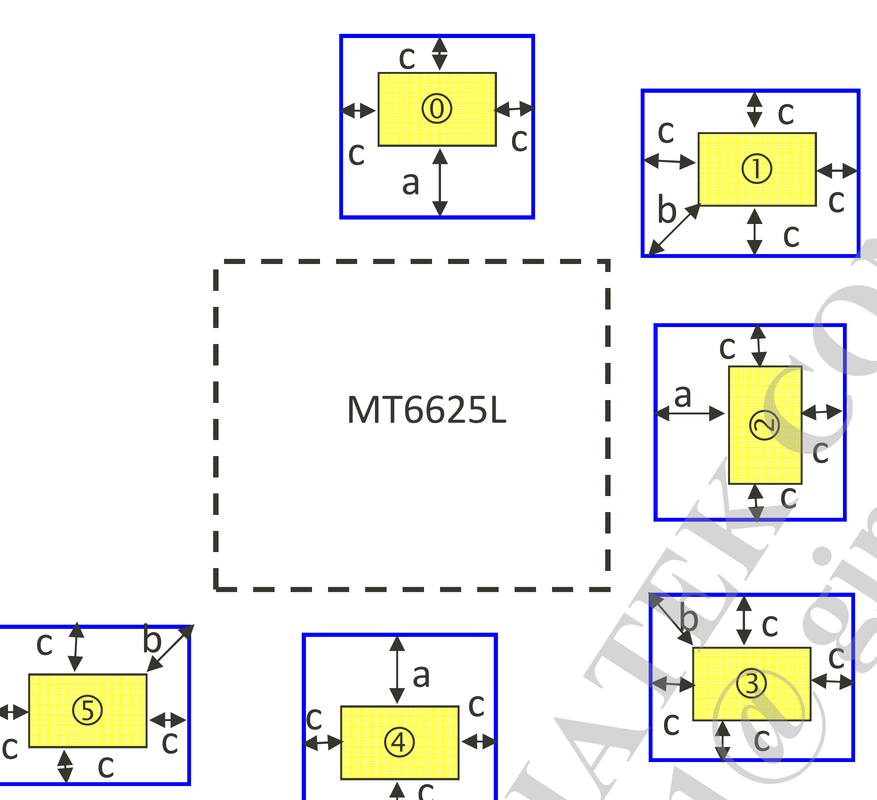
Recommended TCXO Placement



1. ⓪①②③④⑤ are location for TCXO
2. "a ": Isolated GND > 3 mm
3. "b" : Isolated GND > 2 mm
4. "c" : Isolated GND >2 mm

- If the current > 200mA, such as PA, be away from the TCXO > 2cm.
- Other heat sources should be out of blue area.

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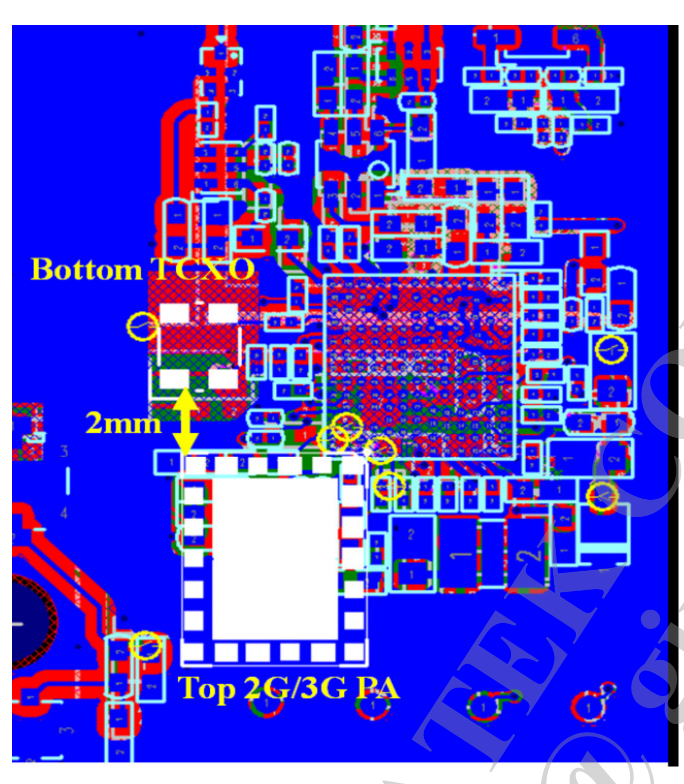
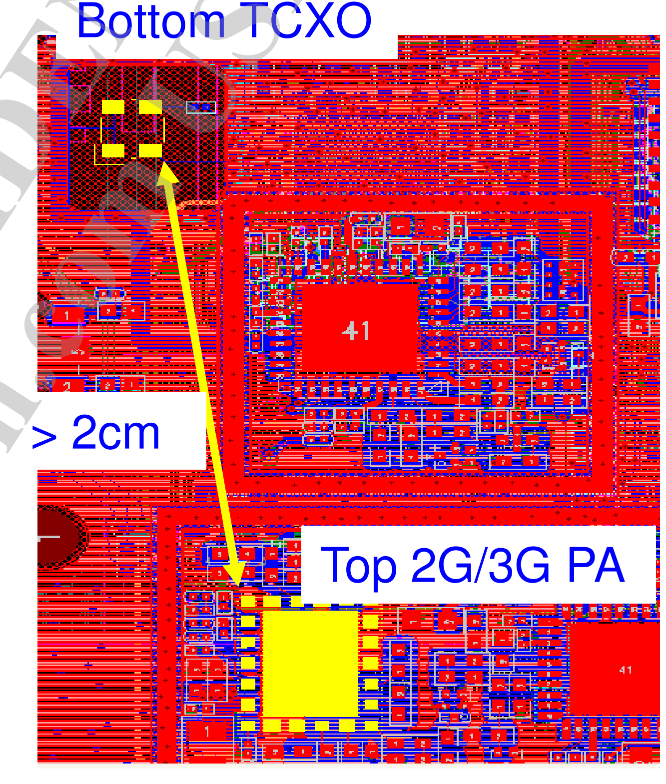
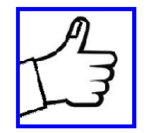
Recommended TCXO Placement (Example)



Bad TCXO Placement





Good TCXO Placement

Far away from PA > 2cm

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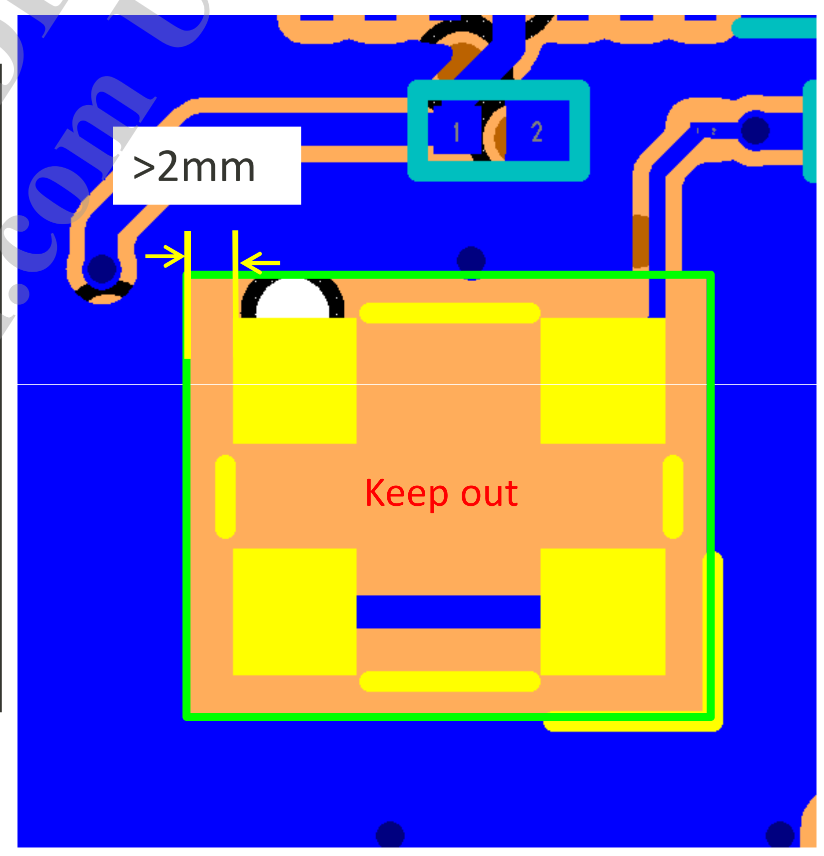
TCXO Wiring Rules

1. TCXO location is the 1st priority of placement. Refer to recommended TCXO placement.
2. The green block region in the figure is the GND plane keep out of TCXO (>2mm).
3. Keep out all layers of this region except for the bottom layer to be far away from the heat source.
4. No signals are allowed to pass the green block region.
5. TCXO clock signal trace must be shielded by GND (adjacent & up/down layers).



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Outlines

- **Brief Introduction to MT6737**
- **Packaging**
  - Package Outline of MT6737
  - MT6737 Footprint Recommendation
  - MT6737 Ball Out Design
- **General Guidelines**
  - PCB Stack-up Recommendation
  - Common Rules and Via Type
  - Placement Notes
  - MT6737 Fan Out
- **Design Guidelines for High-Speed Digital Signals**
  - LPDDR3
  - LPDDR2
  - PDN Design
- **Others**
  - MT6737 RF Interface - MT6169 - MT6158
  - MT6328 (PMU)
  - MT6625 (BT/FM/WiFi/GPS)
  - USB/MIPI/SIM Card/T-Card/eMMC/Differential Pair Layout Suggestion

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USB/MIPI/SIM Card /T-CARD/eMMC /Differential Pair Layout Suggestion

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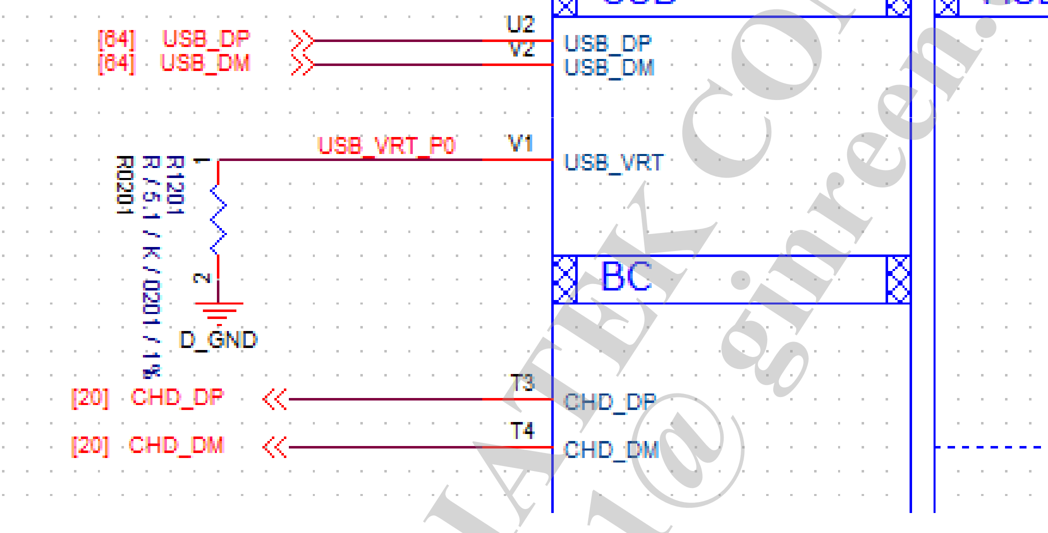
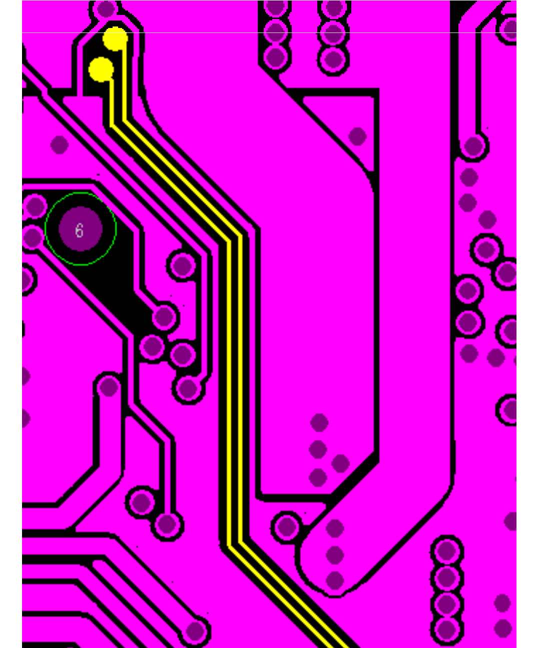
MT6737 USB

- Impedance for USB_DP/DM (differential pair) should be 90Ω with GND shielding.
- Place USB_VRT resistor R1201 close to MT6737.

PCB Net Name	IC Ball	Impedance design
USB_DP_P0	U2	90Ω
USB_DM_P0	V2	
CHD_DP	T3	No impedance; needs GND shielding
CHD_DM	T4	





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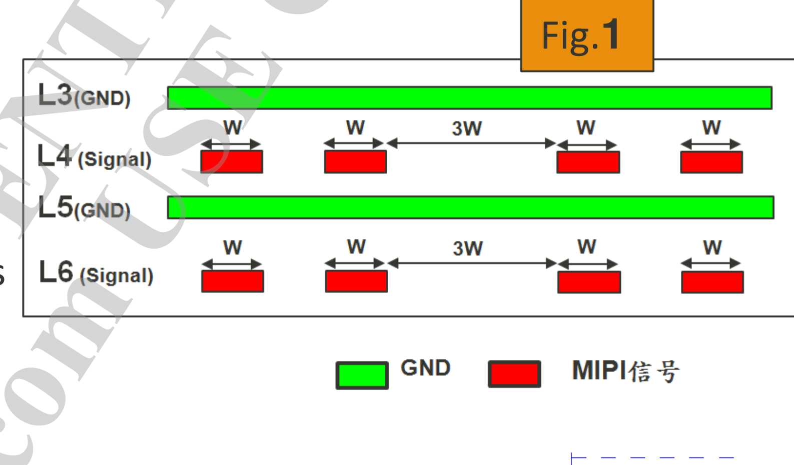
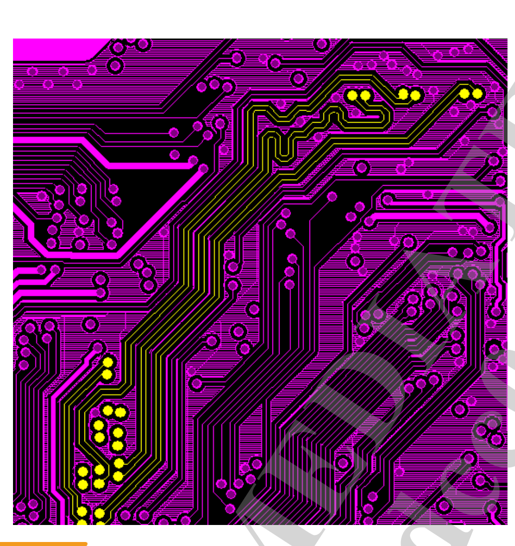
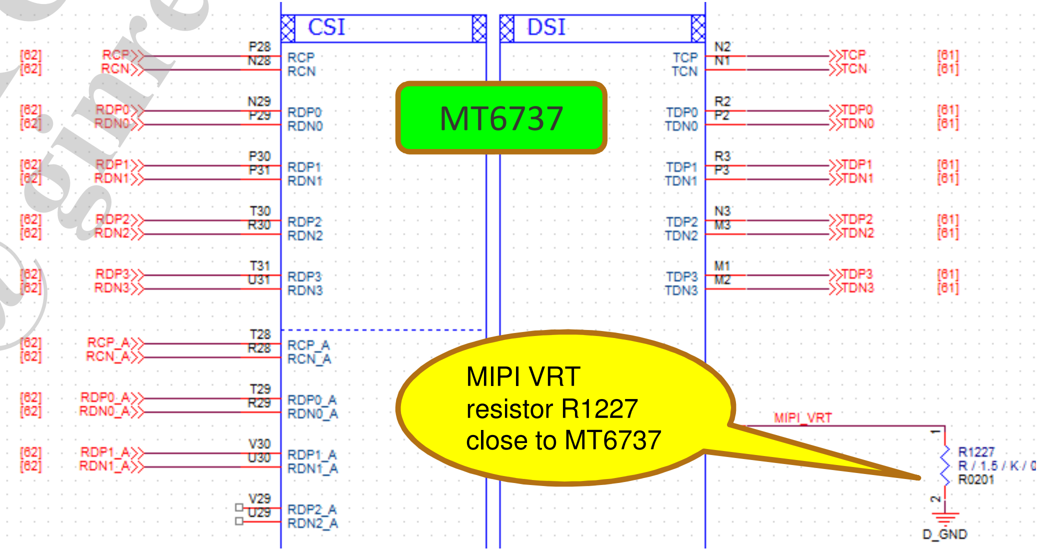
MT6737 MIPI

- MIPI signals' differential impedance: 100Ω
  - TX group: Lane-to-lane matching ≤60mil
  - RX group: Lane-to-lane matching ≤100mil
- Well shielded by GND (adjacent and up/down layers) is recommended; otherwise keep the spacing ≧3W rule (Fig.1)
- CMMCLK: Well shielded by GND (adjacent and up/down layers)
- Place MIPI VRT resistor R1227 close to MT6737.







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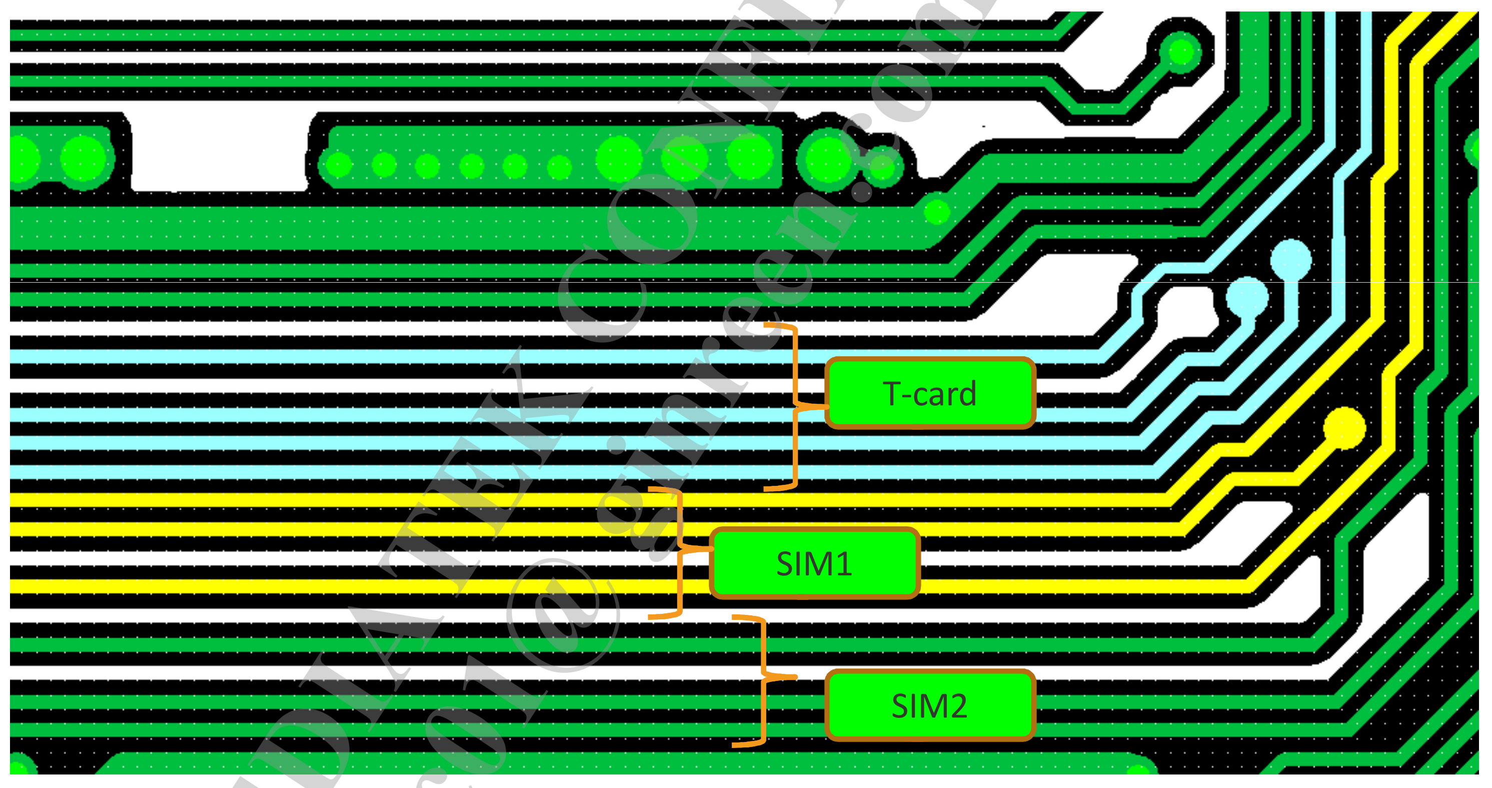
MT6737 SIM & T-CARD

- Route SIM card signals together. SIM1_SCLK/ SIM2_SCLK should be shielded by GND.
- Route T-card signals together. SDC1_CLK should be shielded by GND.



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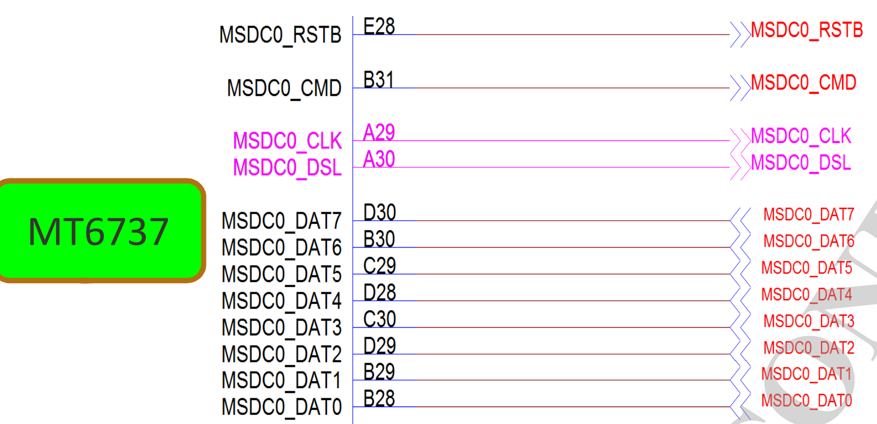
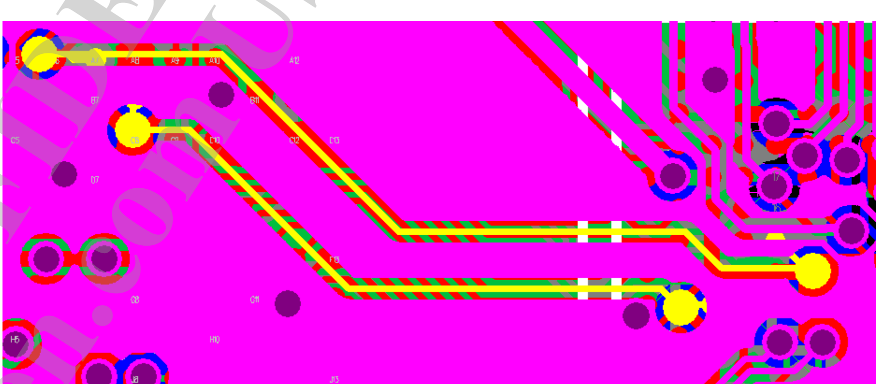
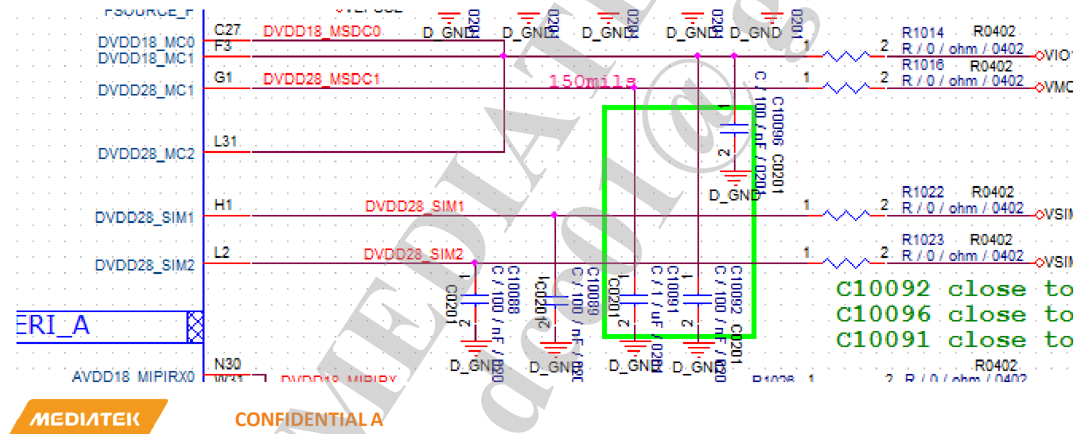
MT6737 eMMC (1/2)

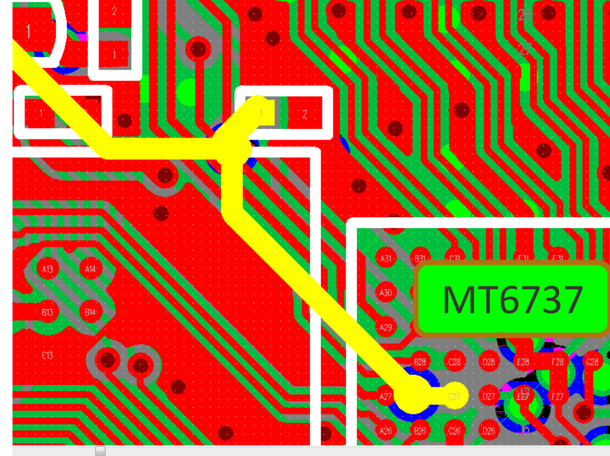
- MSDC0_CLK & MSDC0_DSL should be shielded by GND (adjacent and up/down layers).





- DVDD18_MSDC0 capacitors should be placed near MT6737 pin C27. Decoupling cap. should be placed in 150mil range.





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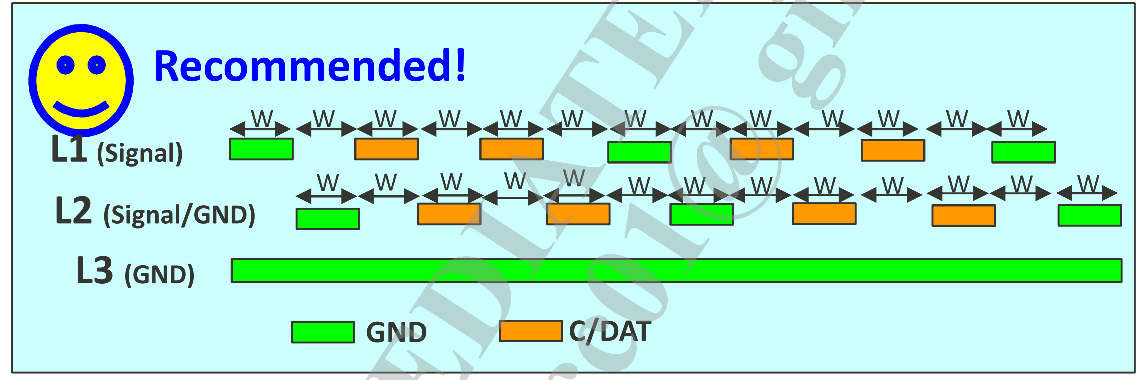
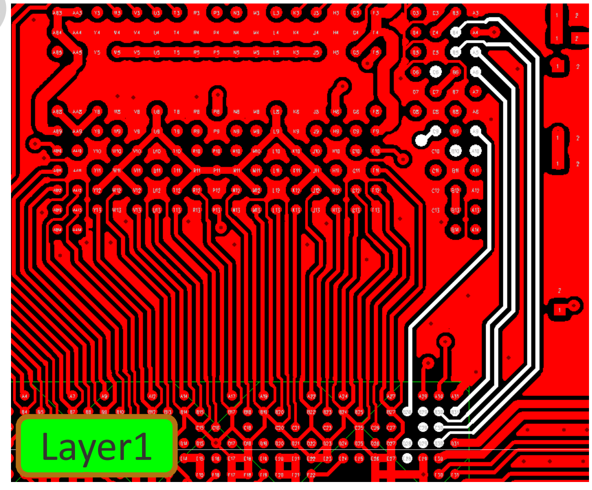
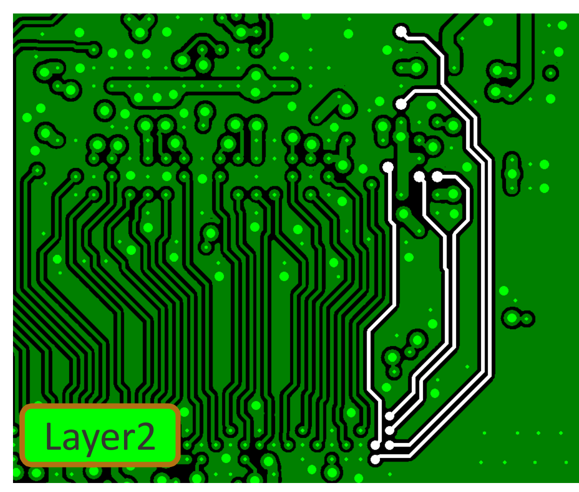
MT6737 eMMC (2/2)

- Route MSDC0_RSTB, MSDC0_CMD, MSDC_DAT0~MSDC_DAT7 at L1 & L2.
- At least route with two trace shielding. Do not overlap at L1 & L2. Overlapping with GND is OK.

Signal	Pin	Net
MSDC0_RSTB	E28	MSDC0_RSTB
MSDC0_CMD	B31	MSDC0_CMD
MSDC0_CLK	A29	MSDC0_CLK
MSDC0_DSL	A30	MSDC0_DSL
MSDC0_DAT7	D30	MSDC0_DAT7
MSDC0_DAT6	B30	MSDC0_DAT6
MSDC0_DAT5	C29	MSDC0_DAT5
MSDC0_DAT4	D28	MSDC0_DAT4
MSDC0_DAT3	C30	MSDC0_DAT3
MSDC0_DAT2	D29	MSDC0_DAT2
MSDC0_DAT1	B29	MSDC0_DAT1
MSDC0_DAT0	B28	MSDC0_DAT0







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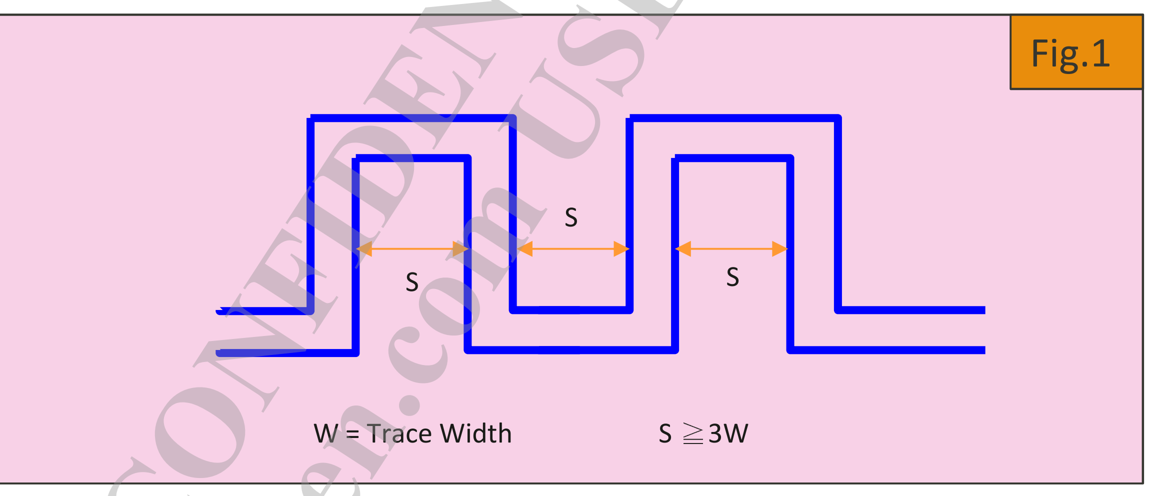
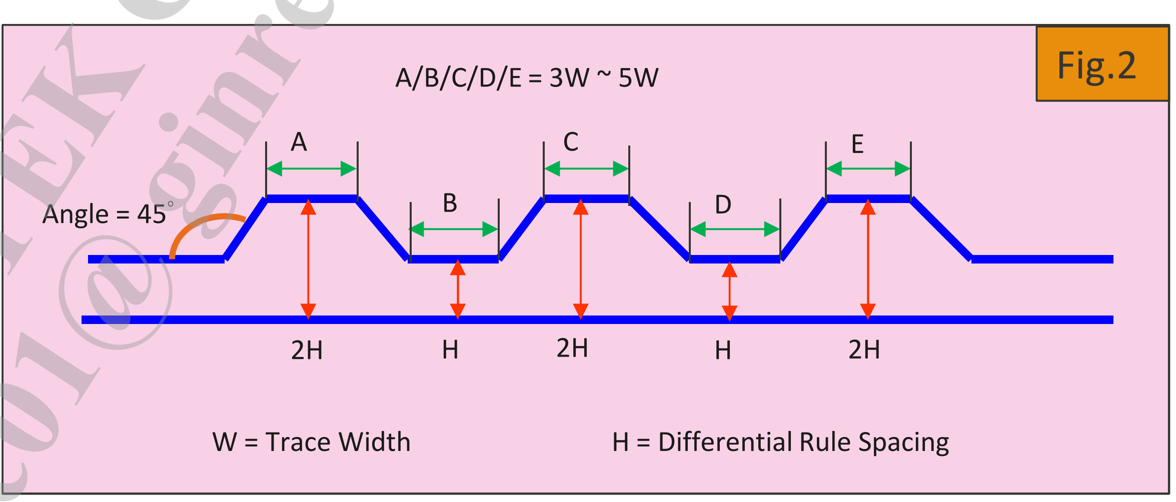
Differential Pair Layout Recommendation

- Keep spacing ≧3W(W=trace width) as Fig.1 when you need to tune both traces for differential pair.



- Follow the suggestion as Fig.2 when you only need to tune single trace for differential pair.



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